

SEG

LCDTV5100

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MODEL

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SERVICE MANUAL

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# **Service Manual**

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**20" Chassis**

**17MB07**

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## 1. INTRODUCTION

20" TFT-LCD TV is a Progressive TV control system based on the  $\mu$ -controller SDA555X, with built-in de-interlacer and scaler.

TFT TV is a progressive scan flicker free colour television with PC input, driving an SVGA(800\*600) panel with 4:3 aspect ratio. The chassis is capable of operation in PAL, SECAM, NTSC (playback) colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L'. Sound system output is supplying 2x3W (10%THD) for left and right outputs of 16 $\Omega$  speakers. The chassis is equipped with two full SCART's, one front-AV, one SVHS, one D-Sub 15 (PC) input, one PC stereo audio input and one line out (left and right) and one HP outputs.

## 2. TUNER

As the thickness of the TV set has a limit, a horizontal mounted tuner is used in the product, which is suitable for CCIR systems B/G, H, L, L', I/I', and D/K. The tuning is available through the digitally controlled I<sup>2</sup>C bus (PLL). Below you will find info on the Tuner in use.

### General description of UV1316:

The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

### Features of UV1316:

1. Member of the UV1300 family small sized UHF/VHF tuners
2. Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
3. Digitally controlled (PLL) tuning via I<sup>2</sup>C-bus
4. Off-air channels, S-cable channels and Hyper band
5. Compact size
6. Complies to "CENELEC EN55020" and "EN55013"

### Pinning:

- |     |                                     |   |                             |
|-----|-------------------------------------|---|-----------------------------|
| 1.  | Gain control voltage (AGC)          | : | 4.0V, Max: 4.5V             |
| 2.  | Tuning voltage                      | : |                             |
| 3.  | I <sup>2</sup> C-bus address select | : | Max: 5.5V                   |
| 4.  | I <sup>2</sup> C-bus serial clock   | : | Min:-0.3V, Max: 5.5V        |
| 5.  | I <sup>2</sup> C-bus serial data    | : | Min:-0.3V, Max: 5.5V        |
| 6.  | Not connected                       | : |                             |
| 7.  | PLL supply voltage                  | : | 5.0V, Min: 4.75V, Max: 5.5V |
| 8.  | ADC input                           | : |                             |
| 9.  | Tuner supply voltage                | : | 33V, Min: 30V, Max: 35V     |
| 10. | Symmetrical IF output 1             | : |                             |
| 11. | Symmetrical IF output 2             | : |                             |

## 3. IF PART (TDA988X)

The TDA9885 is an alignment-free single standard (without positive modulation) vision and sound IF signal PLL.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation including sound AM and FM processing.

Both devices can be used for TV, VTR, PC and set-top box applications.

## 4. MULTI STANDARD SOUND PROCESSOR

The MSP34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x1G has optimum stereo performance without any adjustments.

## 5. AUDIO AMPLIFIER STAGE WITH AN7522

The AN7522 is an audio class-AB amplifier assembled in SIL-12 Pin Plastic Package specially designed for sound cards application. Using this IC chassis operates as a stereo TV set. AN7522 has stand-by feature for low stand-by power consumption and mute feature for pop noise free opening and closing the TV set. It can deliver 2\*3W without clipping at 12V/16 $\Omega$  applications.

## 6. POWER

The LM2576 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 3.0A load with excellent line and load regulation. Two different versions (one having a fixed output voltage of 3.3 V, and one with 5.0 V) of this IC are used in the regulator board.

## 7. MICROCONTROLLER SDA55XX

### 7.1. General Features

- Feature selection via special function register
- Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
- Supply Voltage 2.5 and 3.3 V
- ROM version is used.

### 7.2. External Crystal and Programmable Clock Speed

- Single external 6MHz crystal, all necessary clocks are generated internally
- CPU clock speed selectable via special function registers.
- Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

### 7.3. Microcontroller Features

- 8bit 8051 instruction set compatible CPU.
- 33.33-MHz internal clock (max.)
- 0.360 ms (min.) instruction cycle
- Two 16-bit timers
- Watchdog timer
- Capture compare timer for infrared remote control decoding
- Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
- ADC (4 channels, 8 bit)
- UART (rx, tx)

### 7.4. Memory

- Up to 128 Kilobyte on Chip Program ROM
- Eight 16-bit data pointer registers (DPTR)
- 256-bytes on-chip Processor Internal RAM (IRAM)
- 128bytes extended stack memory.
- Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
- UP to 16KByte on Chip Extended RAM (XRAM) consisting of;
  - 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
  - 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
  - 3-Kilobyte Display Memory

### 7.5. Display Features

- ROM Character set supports all East and West European Languages in single device
- Mosaic Graphic Character Set
- Parallel Display Attributes
- Single/Double Width/Height of Characters
- Variable Flash Rate
- Programmable Screen Size (25 Rows x 33...64 Columns)
- Flexible Character Matrixes (HxV) 12 x 9...16
- Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
- CLUT with up to 4096 colour combinations
- Up to 16 Colours per DRCS Character
- One out of 8 Colours for Foreground and Background Colours for 1-bit DRCS and ROM Characters

#### **7.6. ROM Characters**

- Shadowing
- Contrast Reduction
- Pixel by Pixel Shiftable Cursor With up to 4 Different Colours
- Support of Progressive Scan and 100 Hz.
- 3 X 4Bits RGB-DACs On-Chip
- Free Programmable Pixel Clock from 10 MHz to 32MHz
- Pixel Clock Independent from CPU Clock
- Multinorm H/V-Display Synchronisation in Master or Slave Mode

#### **7.7. Acquisition Features**

- Multistandard Digital Data Slicer
- Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
- Four Different Framing Codes Available
- Data Caption only limited by available Memory
- Programmable VBI-buffer
- Full Channel Data Slicing Supported
- Fully Digital Signal Processing
- Noise Measurement and Controlled Noise Compensation
- Attenuation Measurement and Compensation
- Group Delay Measurement and Compensation
- Exact Decoding of Echo Disturbed Signals

#### **7.8. Ports**

- One 8-bit I/O-port with open drain output and optional I<sup>2</sup>C Bus emulation support (Port0)
- Two 8-bit multifunction I/O-ports (Port1, Port3)
- One 4-bit port working as digital or analogue inputs for the ADC (Port2)
- One 2-bit I/O port with secondary function (P4.2, 4.3, 4.7)
- One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

### **8. SERIAL ACCESS CMOS 16K (2048\*8) EEPROM ST24C16**

The ST24C16 is a 16Kbit electrically erasable programmable memory (EEPROM), organised as 8 blocks of 256\*8 bits. The memory is compatible with the I<sup>2</sup>C standard, two wire serial interface, which uses a bi-directional data bus and serial clock. The memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I<sup>2</sup>C bus definition. This is used together with 1 chip enable input (E) so that up to 2\*8K devices may be attached to the I<sup>2</sup>C bus and selected individually.

### **9. CLASS AB STEREO HEADPHONE DRIVER TDA1308**

The TDA1308 is an integrated class AB stereo headphone driver contained in a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

### **10. SAW FILTERS**

K3953M is an IF Filter for Video Applications. The package is SIP5K. Supported standards are B/G, D/K, I, L/L'.

K9656M is an IF Filter for Audio Applications. The package is SIP5K. Supported standards are B/G, D/K, I, L/L'.

## 11. IC DESCRIPTIONS AND INTERNAL BLOCK DIAGRAM

|            |            |
|------------|------------|
| LM1117     | TDA9885/86 |
| LM2576     | TDA1308T   |
| LM317T     | AN7522N    |
| TFMS5360   | PI5V330    |
| ST24LC21   | GM6015     |
| SST37VF040 | SAA3010T   |
| TEA5114A   | AD9883A    |
| TEA6415    | MC141585   |
| VPC3230D   | MC34063    |
| SDA55XX    | MSP3400G   |

### 11.1. LM1117

#### 11.1.1. General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within  $\pm 1\%$ . The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10 $\mu$ F tantalum capacitor is required at the output to improve the transient response and stability.

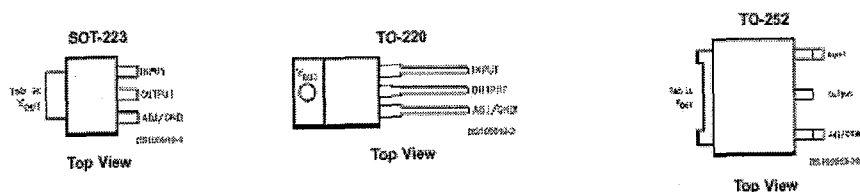
#### 11.1.2. Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
  - LM1117 0°C to 125°C
  - LM1117I -40°C to 125°C

#### 11.1.3. Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

#### 11.1.4. Connection Diagrams



## 11.2. LM2576

### 11.2.1. General Description

The LM2576 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 3.0 A load with excellent line and load regulation.

These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version. These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2576 are offered by several different inductor manufacturers.

Since the LM2576 converter is a switch-mode power supply, its efficiency is significantly higher in comparison with popular three-terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated is so low that no heatsink is required or its size could be reduced dramatically. A standard series of inductors optimized for use with the LM2576 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

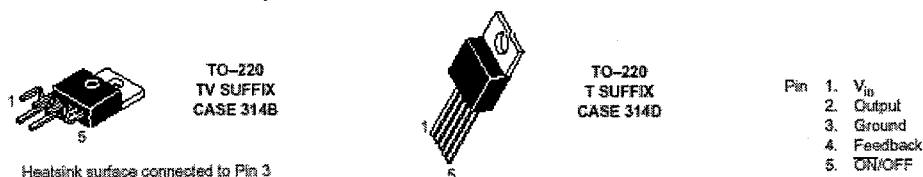
The LM2576 features include a guaranteed  $\pm 4\%$  tolerance on output voltage within specified input voltages and output load conditions, and  $\pm 10\%$  on the oscillator frequency ( $\pm 2\%$  over  $0^\circ\text{C}$  to  $125^\circ\text{C}$ ). External shutdown is included, featuring 80 mA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as

thermal shutdown for full protection under fault conditions.

### 11.2.2. Features

- 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range, 1.23 to 37 V  $\pm 4\%$  Maximum Over Line and Load Conditions
- Guaranteed 3.0 A Output Current
- Wide Input Voltage Range
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- Moisture Sensitivity Level (MSL) Equals 1

### 11.2.3. Pin description



### 11.3. LM317T

#### 11.3.1. Description

The LM317T is an adjustable 3 terminal positive voltage regulator capable of supplying in excess of 1.5 amps over an output range of 1.25 to 37 volts. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof. The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

#### 11.3.2. Features

- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Available in Surface Mount D<sup>2</sup>PAK, and Standard 3-Lead Transistor Package
- Eliminates Stocking many Fixed Voltages

### 11.4. TFMS5360

#### 11.4.1. Description

The TFMS5360 is a miniature receiver for infrared remote control systems.



#### 11.4.2. Features

- Photo detector and preamplifier in one.
- 36 KHZ
- Pin diode and preamp
- IR filter.

## 11.5. ST24LC21

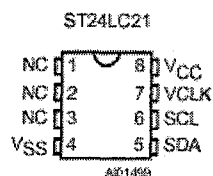
### 11.5.1. Description

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits. This device can operate in two modes: Transmit Only mode and I<sup>2</sup>C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I<sup>2</sup>C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 can not switch from the I<sup>2</sup>C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

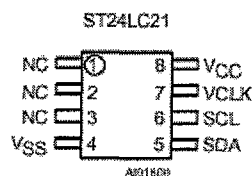
### 11.5.2. Features

- 1 million Erase/Write cycles
- 40 years data retention
- 2.5V to 5.5V single supply voltage
- 400k Hz compatibility over the full range of supply voltage
- Two wire serial interface I<sup>2</sup>C bus compatible
- Page Write (Up To 8 Bytes)
- Byte, random and sequential read modes
- Self timed programming cycle
- Automatic address incrementing
- Enhanced ESD/Latch up
- Performances

### 11.5.3. Pin connections



DIP Pin connections



CO Pin connections

NC: Not connected

#### Signal names

|                 |                                      |
|-----------------|--------------------------------------|
| SDA             | Serial data Address Input/Output     |
| SCL             | Serial Clock (I <sup>2</sup> C mode) |
| V <sub>cc</sub> | Supply voltage                       |
| V <sub>ss</sub> | Ground                               |
| VCLK            | Clock transmit only mode             |

## 11.6. SST37VF040

### 11.6.1. Description

The SST37VF512/010/020/040 devices are 64K x8 / 128Kx8 / 256K x8 / 512K x8 CMOS, Many-Time Programmable (MTP), low cost flash, manufactured with SST's proprietary, high performance CMOS Super Flash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST37VF512/010/020/040 can be electrically erased and programmed at least 1000 times using an external programmer, e.g., to change the contents of devices in inventory. The SST37VF512/010/020/040 have to be erased prior to programming. These devices conform to JEDEC standard pinouts for byte-wide flash memories. Featuring high performance Byte-Program, the SST37VF512/010/020/040 provide a typical Byte-Program time of 10  $\mu$ s. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with an endurance of at least 1000 cycles. Data retention is rated at greater than 100 years. The SST37VF512/010/020/040 are suited for applications that require infrequent writes and low power nonvolatile storage. These devices will improve flexibility, efficiency and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

### 11.6.2. Features

- Organized as 64K x8 / 128K x8 / 256K x8 / 512K x8
- 2.7-3.6V Read Operation
- Superior Reliability
  - Endurance: At least 1000 Cycles
  - Greater than 100 years Data Retention
- Low Power Consumption:
  - Active Current: 10 mA (typical)
  - Standby Current: 2  $\mu$ A (typical)
- Fast Read Access Time:
  - 70 ns
  - 90 ns
- Latched Address and Data
- Fast Byte-Program Operation:
  - Byte-Program Time: 10  $\mu$ s (typical)
  - Chip Program Time:
    - 0.6 seconds (typical) for SST37VF512
    - 1.2 seconds (typical) for SST37VF010
    - 2.4 seconds (typical) for SST37VF020
    - 4.8 seconds (typical) for SST37VF040
- Electrical Erase Using Programmer
  - Does not require UV source
  - Chip-Erase Time: 100 ms (typical)
- CMOS I/O Compatibility
- JEDEC Standard Byte-wide Flash EEPROM Pinouts
- Packages Available
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
  - 32-pin PDIP

### 11.6.3. Pin Description

| Symbol            | Pin name          | Functions                                                                                                                             |
|-------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| $A_{MS} - A_0$    | Address Inputs    | To provide memory addresses.                                                                                                          |
| $D_{Q7} - D_{Q0}$ | Data Input/output | To output data during Read cycles and receive input data during Program cycles. The outputs are in tri-state when OE# or CE# is high. |
| CE#               | Chip Enable       | To activate the device when CE# is low.                                                                                               |
| WE#               | Write Enable      | To program or erase (WE# = VIL pulse during Program or Erase)                                                                         |
| OE#               | Output Enable     | To gate the data output buffers during Read operation when low                                                                        |
| $V_{DD}$          | Power Supply      | To provide 3.0V supply (2.7-3.6V)                                                                                                     |
| $V_{SS}$          | Ground            |                                                                                                                                       |
| NC                | No Connection     | Unconnected pins.                                                                                                                     |

1.  $A_{MS}$  = Most significant address

$A_{MS}$  =  $A_{15}$  for SST37VF512,  $A_{16}$  for SST37VF010,  $A_{17}$  for SST37VF020, and  $A_{18}$  for SST37VF040

## 11.7. TEA5114A

### 11.7.1. General description

This integrated circuit provides RGB switching allowing connections between peri TV plug, internal RGB generator and video processor in a TV set.

The input signal black level is tied to the same reference voltage on each input in order to have no differential voltage when switching two RGB generators.

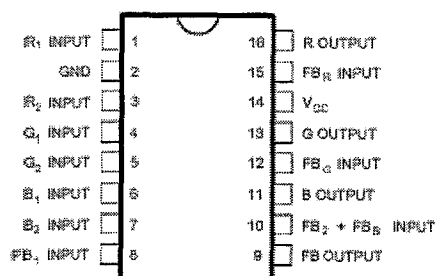
An AC output signal higher than 2 Vpp makes gain going slowly down to 0dB to protect the TV set video amplifier from saturation.

Fast blanking output is a logical OR between FB1 (Pin 8) and FB2 (Pin 10).

### 11.7.2. Features

- 25MHz Bandwidth
- Crosstalk : 55dB
- Short circuit to ground or Vcc protected
- Anti saturation gain changing
- Video switching

### 11.7.3. Pin Connections



## 11.8. TEA6415

### 11.8.1. General description

The main function of the IC is to switch 8 video input sources on 6 outputs. Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals). Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 Vdc on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS. Driving 75Ω load needs an external transistor. It is possible to have the same input connected to several outputs. The starting configuration upon power on (power supply: 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

### 11.8.2. 13.5.2.Features

- 20MHz Bandwidth
- Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
- 8 Inputs (CVBS, RGB, MAC, CHROMA,...)
- 6 Outputs
- Possibility of MAC or chroma signal for each input by switching-off the clamp with an external resistor bridge
- Bus controlled
- 6.5dB gain between any input and output
- 55dB crosstalk at 5mHz
- Fully ESD protected

### 11.8.3. 13.5.3.Pinning

|     |        |   |                      |                                      |                  |
|-----|--------|---|----------------------|--------------------------------------|------------------|
| 1.  | Input  | : | Max                  | : 2Vpp, Input Current: 1mA, Max: 3mA |                  |
| 2.  | Data   | : | Low level            | : -0.3V Max: 1.5V,                   |                  |
|     |        |   | High level           | : 3.0V Max : Vcc+0.5V                |                  |
| 3.  | Input  | : | Max                  | : 2Vpp, Input Current: 1mA, Max      | : 3mA            |
| 4.  | Clock  | : | Low level            | : -0.3V Max: 1.5V,                   |                  |
|     |        |   | High level           | : 3.0V Max : Vcc+0.5V                |                  |
| 5.  | Input  | : | Max                  | : 2Vpp, Input Current: 1mA, Max: 3mA |                  |
| 6.  | Input  | : | Max                  | : 2Vpp, Input Current: 1mA, Max: 3mA |                  |
| 7.  | Prog   | : |                      |                                      |                  |
| 8.  | Input  | : | Max                  | : 2Vpp, Input Current: 1mA, Max: 3mA |                  |
| 9.  | Vcc    | : | 12V                  |                                      |                  |
| 10. | Input  | : | Max                  | : 2Vpp, Input Current: 1mA, Max: 3mA |                  |
| 11. | Input  | : | Max                  | : 2Vpp, Input Current: 1mA, Max: 3mA |                  |
| 12. | Ground | : |                      |                                      |                  |
| 13. | Output | : | 5.5Vpp,              | Min : 4.5Vpp                         |                  |
| 14. | Output | : | 5.5Vpp,              | Min : 4.5Vpp                         |                  |
| 15. | Output | : | 5.5Vpp,              | Min : 4.5Vpp                         |                  |
| 16. | Output | : | 5.5Vpp,              | Min : 4.5Vpp                         |                  |
| 17. | Output | : | 5.5Vpp,              | Min : 4.5Vpp                         |                  |
| 18. | Output | : | 5.5Vpp, Min : 4.5Vpp |                                      |                  |
| 19. | Ground | : |                      |                                      |                  |
| 20. | Input  | : | Max                  | : 2Vpp, Input Current                | : 1mA, Max : 3mA |

## 11.9. VPC3230D

### 11.9.1. General Description

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 323xD are

- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard colour decoder PAL/NTSC/SECAM including all substandards
- four CVBS, one S-VHS input, one CVBS output
- two RGB/YCrCb component inputs, one Fast Blank (FB) input
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling 'Panorama-vision'
- PAL+ preprocessing
- line-locked clock, data and sync, or 656-output interface
- peaking, contrast, brightness, color saturation and tint for RGB/ YCrCb and CVBS/ S-VHS
- high-quality soft mixer controlled by Fast Blank
- PIP processing for four picture sizes (1/4, 1/9, 1/16 or 1/36 of normal size) with 8-bit resolution
- 15 predefined PIP display configurations and expert mode (fully programmable)
- control interface for external field memory
- I<sup>2</sup>C-bus interface
- one 20.25-MHz crystal, few external components
- 80-pin PQFP package

### 11.9.2. Pin Connections and Short Descriptions

NC = not connected

LV = if not used, leave vacant

X = obligatory; connect as described in circuit diagram

SUPPLYA = 4.75...5.25 V, SUPPLYD = 3.15...3.45 V

| Pin No.<br>PQFP<br>80-pin | Pin Name            | Type    | Connection<br>(if not used) | Short Description                           |
|---------------------------|---------------------|---------|-----------------------------|---------------------------------------------|
| 1                         | B1/CB1IN            | IN      | VREF                        | Blue1/Cb1 Analog Component Input            |
| 2                         | G1/Y1IN             | IN      | VREF                        | Green1/Y1 Analog Component Input            |
| 3                         | R1/CR1IN            | IN      | VREF                        | Read1/Cr1 Analog Component Input            |
| 4                         | B2/CB2IN            | IN      | VREF                        | Blue2/Cb2 Analog Component Input            |
| 5                         | G2/Y2IN             | IN      | VREF                        | Green2/Y2 Analog Component Input            |
| 6                         | R2/CR2IN            | IN      | VREF                        | Read2/Cr2 Analog Component Input            |
| 7                         | ASGF                |         | X                           | Analog Shield GND <sub>F</sub>              |
| 8                         | FFRSTWIN            | IN      | LV or GND <sub>D</sub>      | FIFO Reset Write Input                      |
| 9                         | V <sub>SUPCAP</sub> | OUT     | X                           | Digital Decoupling Circuitry Supply Voltage |
| 10                        | V <sub>SUPD</sub>   | SUPPLYD | X                           | Supply Voltage, Digital Circuitry           |
| 11                        | GND <sub>D</sub>    | SUPPLYD | X                           | Ground, Digital Circuitry                   |
| 12                        | GND <sub>CAP</sub>  | OUT     | X                           | Digital Decoupling Circuitry GND            |
| 13                        | SCL                 | IN/OUT  | X                           | I <sup>2</sup> C Bus Clock                  |
| 14                        | SDA                 | IN/OUT  | X                           | I <sup>2</sup> C Bus Data                   |
| 15                        | RESQ                | IN      | X                           | Reset Input, Active Low                     |
| 16                        | TEST                | IN      | GND <sub>D</sub>            | Test Pin, connect to GND <sub>D</sub>       |
| 17                        | VGAV                | IN      | GND <sub>D</sub>            | VGAV Input                                  |
| 18                        | YCOEQ               | IN      | GND <sub>D</sub>            | Y/C Output Enable Input, Active Low         |
| 19                        | FFIE                | OUT     | LV                          | FIFO Input Enable                           |
| 20                        | FFWE                | OUT     | LV                          | FIFO Write Enable                           |
| 21                        | FFRSTW              | OUT     | LV                          | FIFO Reset Write/Read                       |
| 22                        | FFRE                | OUT     | LV                          | FIFO Read Enable                            |
| 23                        | FFOE                | OUT     | LV                          | FIFO Output Enable                          |
| 24                        | CLK20               | IN/OUT  | LV                          | Main Clock output 20.25 MHz                 |
| 25                        | GND <sub>PA</sub>   | OUT     | X                           | Pad Decoupling Circuitry GND                |
| 26                        | V <sub>SUPPA</sub>  | OUT     | X                           | Pad Decoupling Circuitry Supply Voltage     |
| 27                        | LLC2                | OUT     | LV                          | Double Clock Output                         |
| 28                        | LLC1                | IN/OUT  | LV                          | Clock Output                                |
| 29                        | V <sub>SUPLLC</sub> | SUPPLYD | X                           | Supply Voltage, LLC Circuitry               |

|    |                    |         |                        |                                                                         |
|----|--------------------|---------|------------------------|-------------------------------------------------------------------------|
| 30 | GND <sub>LLC</sub> | SUPPLYD | X                      | Ground, LLC Circuitry                                                   |
| 31 | Y7                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma (MSB)                                                  |
| 32 | Y6                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma                                                        |
| 33 | Y5                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma                                                        |
| 34 | Y4                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma                                                        |
| 35 | GND <sub>y</sub>   | SUPPLYD | X                      | Ground, Luma Output Circuitry                                           |
| 36 | V <sub>SUPY</sub>  | SUPPLYD | X                      | Supply Voltage, Luma Output Circuitry                                   |
| 37 | Y3                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma                                                        |
| 38 | Y2                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma                                                        |
| 39 | Y1                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma                                                        |
| 40 | Y0                 | OUT     | GND <sub>y</sub>       | Picture Bus Luma (LSB)                                                  |
| 41 | C7                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma (MSB)                                                |
| 42 | C6                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma                                                      |
| 43 | C5                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma                                                      |
| 44 | C4                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma                                                      |
| 45 | V <sub>SUPC</sub>  | SUPPLYD | X                      | Supply Voltage, Chroma Output Circuitry                                 |
| 46 | GND <sub>c</sub>   | SUPPLYD | X                      | Ground, Chroma Output Circuitry                                         |
| 47 | C3                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma                                                      |
| 48 | C2                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma                                                      |
| 49 | C1                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma                                                      |
| 50 | C0                 | OUT     | GND <sub>c</sub>       | Picture Bus Chroma (LSB)                                                |
| 51 | GND <sub>SY</sub>  | SUPPLYD | X                      | Ground Sync Pad Circuitry                                               |
| 52 | V <sub>SUPSY</sub> | SUPPLYD | X                      | Supply Voltage, Sync Pad Circuitry                                      |
| 53 | INTLC              | OUT     | LV                     | Interlace Output                                                        |
| 54 | AVO                | OUT     | LV                     | Active Video Output                                                     |
| 55 | FSY/HG/HSYA        | OUT     | LV                     | Front Sync/ Horizontal Clamp Pulse/Front-End Horizontal Sync Output     |
| 56 | MSY/HS             | IN/OUT  | LV                     | Main Sync/Horizontal Sync Pulse                                         |
| 57 | VS                 | OUT     | LV                     | Vertical Sync Pulse                                                     |
| 58 | FPDAT/VSYA         | IN/OUT  | LV                     | Front End/Back-End Data/Front-End Vertical Sync Output                  |
| 59 | V <sub>STBY</sub>  | SUPPLYA | X                      | Standby Supply Voltage                                                  |
| 60 | CLK5               | OUT     | LV                     | CCU 5 MHz Clock Output                                                  |
| 61 | NC                 | -       | LV or GND <sub>o</sub> | Not Connected                                                           |
| 62 | XTAL1              | IN      | X                      | Analog Crystal Input                                                    |
| 63 | XTAL2              | OUT     | X                      | Analog Crystal Output                                                   |
| 64 | ASGF               |         | X                      | Analog Shield GND <sub>f</sub>                                          |
| 65 | GND <sub>f</sub>   | SUPPLYA | X                      | Ground, Analog Front-End                                                |
| 66 | VRT                | OUTPUT  | X                      | Reference Voltage Top, Analog                                           |
| 67 | I2CSEL             | IN      | X                      | I <sup>2</sup> C Bus Address Select                                     |
| 68 | ISGND              | SUPPLYA | X                      | Signal Ground for Analog Input, connect to GND <sub>f</sub>             |
| 69 | V <sub>SUPF</sub>  | SUPPLYA | X                      | Supply Voltage, Analog Front-End                                        |
| 70 | VOU                | OUT     | LV                     | Analog Video Output                                                     |
| 71 | CIN                | IN      | LV                     | Chroma/Analog Video 5 Input                                             |
| 72 | VIN1               | IN      | VRT                    | Video 1 Analog Input                                                    |
| 73 | VIN2               | IN      | VRT                    | Video 2 Analog Input                                                    |
| 74 | VIN3               | IN      | VRT                    | Video 3 Analog Input                                                    |
| 75 | VIN4               | IN      | VRT                    | Video 4 Analog Input                                                    |
| 76 | V <sub>SUPAI</sub> | SUPPLYA | X                      | Supply Voltage, Analog Component Inputs Front-End                       |
| 77 | GND <sub>AI</sub>  | SUPPLYA | X                      | Ground, Analog Component Inputs Front-End                               |
| 78 | VREF               | OUTPUT  | X                      | Reference Voltage Top, Analog Component Inputs Front-End                |
| 79 | FB1IN              | IN      | VREF                   | Fast Blank Input                                                        |
| 80 | AISGND             | SUPPLYA | X                      | Signal Ground for Analog Component Inputs, connect to GND <sub>AI</sub> |

## 11.10. SDA55XX (SDA5550)

### 11.10.1. General description

The SDA55XX is a single chip teletext decoder for decoding World System Teletext data as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide Screen Signalling (WSS) data used for PAL plus transmissions (Line 23). The device also supports Closed caption acquisition and decoding. The device provides an integrated general-purpose, fully 8051-compatible Microcontroller with television specific hardware features. Microcontroller has been enhanced to provide powerful features such as memory banking, data pointers, and additional interrupts etc. The on-chip display unit for displaying Level 1.5 teletext data can also be used for customer defined on screen displays. Internal XRAM consists of up to 16 Kbytes. Device has an internal ROM of up to 128 KBytes. ROMless versions can access up to 1 MByte of external RAM and ROM. The SDA 55XX supports a wide range of standards including PAL, NTSC and contains a digital slicer for VPS, WSS, PDC, TTX and Closed Caption, an accelerating acquisition hardware module, a display generator for Level 1.5 TTX data and powerful On screen Display capabilities based on parallel attributes, and Pixel oriented characters (DRCS).

The 8-bit Microcontroller runs at 360 ns. cycle time (min.). Controller with dedicated hardware does most of the internal TTX acquisition processing, transfers data to/from external memory interface and receives/transmits data via I<sup>2</sup>C-firmware user-interface. The slicer combined with dedicated hardware stores TTX data in a VBI buffer of 1 Kilobyte. The Microcontroller firmware performs all the acquisition tasks (hamming and parity-checks, page search and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26-handling, FLOF, TOP and list-pages. The interface to user software is optimized for minimal overhead. SDA 55XX is realized in 0.25 micron technology with 2.5 V supply voltage and 3.3 V I/O (TTL compatible). The software and hardware development environment (TEAM) is available to simplify and speed up the development of the software and On Screen Display. TEAM stands for TVT Expert Application Maker. It improves the TV controller software quality in following aspects:

- Shorter time to market
- Re-usability
- Target independent development
- Verification and validation before targeting
- General test concept
- Graphical interface design requiring minimum programming and controller know how.
- Modular and open tool chain, configurable by customer.

## 11.11. TDA9885/86

### 11.11.1. General description

The TDA9885 is an alignment-free single standard (without positive modulation) vision and sound IF signal PLL. The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation including sound AM and FM processing. Both devices can be used for TV, VTR, PC and set-top box applications.

### 11.11.2. Features

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
- Multistandard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Gated phase detector for L/L accent standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative and positive modulated standards via I<sup>2</sup>C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz
- 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter; AFC bits via I<sup>2</sup>C-bus readable
- TakeOver Point (TOP) adjustable via I<sup>2</sup>C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode (PLL controlled)
- SIF AGC for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I<sup>2</sup>C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- I<sup>2</sup>C-bus control for all functions
- I<sup>2</sup>C-bus transceiver with pin programmable Module Address (MAD).

### 11.11.3. Pinning

| SYMBOL         | PIN | DESCRIPTION                                        |
|----------------|-----|----------------------------------------------------|
| VIF1           | 1   | VIF differential input 1                           |
| VIF2           | 2   | VIF differential input 2                           |
| OP1            | 3   | output 1 (open-collector)                          |
| FMPLL          | 4   | FM-PLL for loop filter                             |
| DEEM           | 5   | de-emphasis output for capacitor                   |
| AFD            | 6   | AF decoupling input for capacitor                  |
| DGND           | 7   | digital ground                                     |
| AUD            | 8   | audio output                                       |
| TOP            | 9   | tuner AGC TakeOver Point (TOP)                     |
| SDA            | 10  | I <sup>2</sup> C-bus data input/output             |
| SCL            | 11  | I <sup>2</sup> C-bus clock input                   |
| SIOMA          | 12  | sound intercarrier output and MAD select           |
| n.c.           | 13  | not connected                                      |
| TAGC           | 14  | tuner AGC output                                   |
| REF            | 15  | 4 MHz crystal or reference input                   |
| VAGC           | 16  | VIF-AGC for capacitor; (Not connected for TDA9885) |
| CVBS           | 17  | video output                                       |
| AGND           | 18  | analog ground                                      |
| VPLL           | 19  | VIF-PLL for loop filter                            |
| V <sub>p</sub> | 20  | supply voltage (+5 V)                              |
| AFC            | 21  | AFC output                                         |
| OP2            | 22  | output 2 (open-collector)                          |
| SIF1           | 23  | SIF differential input 1                           |
| SIF2           | 24  | SIF differential input 2                           |

## 11.12. TDA1308

### 11.12.1. General Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

### 11.12.2. Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
- high signal-to-noise ratio
- High slew rate
- Low distortion
- Large output voltage swing.

### 11.12.3. Pinning

| SYMBOL          | PIN | DESCRIPTION              | PIN VALUE                  |
|-----------------|-----|--------------------------|----------------------------|
| OUTA            | 1   | Output A (Voltage swing) | Min : 0.75V, Max : 4.25V   |
| INA(neg)        | 2   | Inverting input A        | Vo(clip) : Min : 1400mVrms |
| INA(pos)        | 3   | Non-inverting input A    | 2.5V                       |
| V <sub>ss</sub> | 4   | Negative supply          | 0V                         |
| INB(pos)        | 5   | Non-inverting input B    | 2.5V                       |
| INB(neg)        | 6   | Inverting input B        | Vo(clip) : Min : 1400mVrms |
| OUTB            | 7   | Output B (Voltage swing) | Min : 0.75V, Max : 4.25V   |
| V <sub>DD</sub> | 8   | Positive supply          | 5V, Min : 3.0V, Max : 7.0V |

## 11.13. AN7522N

### 11.13.1. General description

AN7522N is a BTL 5.0W x 2ch Power Amplifier with Standby and Volume Function Silicon Monolithic Bipolar IC. It is used for low frequency amplifier applications.

### 11.13.2. Pin Descriptions

| Pin No | Description       | Pin No | Description       |
|--------|-------------------|--------|-------------------|
| 1      | Vcc               | 7      | GND (Input)       |
| 2      | Ch.1 Output (+)   | 8      | Ch.2 Input        |
| 3      | GND (Ch.1 Output) | 9      | Volume            |
| 4      | Ch.1 Output (-)   | 10     | Ch.2 Output (-)   |
| 5      | Standby           | 11     | GND (Ch.2 Output) |
| 6      | Ch.1 Input        | 12     | Ch.2 Output (+)   |

## 11.14. PI5V330

### 11.14.1. General description

Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance.

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch™ can be driven from a current output RAMDAC or voltage output composite video source.

Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation.

The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

### 11.14.2. Features

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3V
- Low crosstalk at 10 MHz: -58 dB
- Ultra-low quiescent power (0.1  $\mu$ A typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
  - 16-pin 300-mil wide plastic SOIC (S)
  - 16-pin 150-mil wide plastic SOIC (W)
  - 16-pin 150-mil wide plastic QSOP (Q)

### 11.14.3. Pin Descriptions

| Pin Name                                                                                                                                         | Description      |
|--------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| S1 <sub>A</sub> , S2 <sub>A</sub><br>S1 <sub>B</sub> , S2 <sub>B</sub><br>S1 <sub>C</sub> , S2 <sub>C</sub><br>S1 <sub>D</sub> , S2 <sub>D</sub> | Analog Video I/O |
| IN                                                                                                                                               | Select Input     |
| EN                                                                                                                                               | Enable           |
| D <sub>A</sub> , D <sub>B</sub> ,<br>D <sub>C</sub> , D <sub>D</sub>                                                                             | Analog Video I/O |
| GND                                                                                                                                              | Ground           |
| V <sub>CC</sub>                                                                                                                                  | Power            |

## 11.15. GM6015

### 11.15.1. General description

The Genesis Microchip 6015RD1 LCD TV reference board is a complete display processor for LCD, PDP and LCOS based televisions. The reference board demonstrates the processing capabilities of the Genesis Microchip gm6015 television controller IC. The gm6015 IC is a full-featured, dual-channel video processor with Genesis industry leading Crystal Ciema Plus™ video scan conversion. The 6015RD1 board inputs analog YPbPr/RGB, NTSC/PAL/SECAM CVBS/YC, UHF/VHF and outputs digital RGB to an XGA LCD panel. A convenient on-screen display system provides easy control of the board's processing capabilities. The design kit is complete with hardware and software. Software includes G-Probe debug software, G-Wizard register calculator and G-TV application source code. The 6015RD1 is a related reference board that outputs analog YpbPr/RGB.

### 11.15.2. Features

- Dual channel, gm6015 based LCD TV system
- Industry leading Crystal Cinema Plus video scan conversion
- Inputs:
  - i. Component analog YPbPr/RGB
  - ii. 480/576I, 480/576P, 720P and 1080I HD
  - iii. Dual NTSC/PAL/SECAM CVBS and YC
  - iv. VGA, SVGA, XGA PC graphics
  - v. Separate, composite or sync on Y/G
  - vi. UHF/VHF RF (NTSC)
- Default output with XGA LCD interface PCB:
  - i. Component analog YpbPr/RGB
- Other outputs:
  - ii. 8/16/20/24-bit 4:2:2/4:4:4 digital YCbCr/RGB
  - iii. 480/576I, 480/576P, 720P and 1080I HD
  - iv. VGA, SVGA, XGA PC graphics
  - v. Separate, composite or sync on Y/G
- On-screen display (OSD) user interface with automated self running demonstration
- Small form factor PCB

## 11.16. SAA3010T

### 11.16.1. Description

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section "Keyboard operation".

### 11.16.2. Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

### 11.16.3. Pinning

| Pin   | Mnemonic       | Function                                                                                |
|-------|----------------|-----------------------------------------------------------------------------------------|
| 1     | X7 (IPU)       | Sense input from key matrix                                                             |
| 2     | SSM (I)        | Sense mode selection input                                                              |
| 3     | Z0-Z3 (IPU)    | Sense inputs from key matrix                                                            |
| 7     | MDATA (OP3)    | Generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor |
| 8     | DATA (OP3)     | Generated output information                                                            |
| 9-13  | DR7-DR3 (ODN)  | Scan drivers                                                                            |
| 14    | VSS            | Ground (0V)                                                                             |
| 15-17 | DR-2-DR0 (ODN) | Scan drivers                                                                            |
| 18    | OSC (I)        | Oscillator input                                                                        |
| 19    | TP2 (I)        | Test point 2                                                                            |
| 20    | TP1 (I)        | Test point 1                                                                            |
| 21-27 | X0-X6 (IPU)    | Sense inputs from key matrix                                                            |
| 28    | VDD(I)         | Voltage supply                                                                          |

**Note:**

(I): Input,

(IPU): input with p-channel pull-up transistor,

(ODN): output with open drain n-channel transistor

(OD3): output 3-state

## 11.17. AD9883A

### 11.17.1. General description

The AD9883A is a complete 8-bit, 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 1024 at 75 Hz).

The AD9883A includes a 140 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883A's on-chip PLL generates a pixel clock from the Hsync input. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of Hsync. A sampling phase adjustment is provided. Data, Hsync, and clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

### 11.17.2. Features

- 140 MSPS Maximum Conversion Rate
- 300 MHz Analog Bandwidth
- 0.5 V to 1.0 V Analog Input Range
- 500 ps p-p PLL Clock Jitter at 110 MSPS
- 3.3 V Power Supply
- Full Sync Processing
- Sync Detect for "Plugging"
- Midscale Clamping
- Power-Down Mode
- Low Power: 500 mW Typical
- 4:2:2 Output Format Mode

### 11.17.3. Pin Descriptions

| Pin Name                        | Function                                                                                                                                                                                                                                                                                                                                    |
|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>OUTPUTS</b>                  |                                                                                                                                                                                                                                                                                                                                             |
| HSOUT                           | Horizontal Sync Output<br>A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATAACK and Data, data timing with respect to horizontal sync can always be determined.                                     |
| VSOUT                           | Vertical Sync Output<br>A reconstructed and phase-aligned version of the video Vsync. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.                                                                                                       |
| SOGOUT                          | Sync-On-Green Slicer Output<br>This pin outputs either the signal from the Sync-on-Green slicer comparator or an unprocessed but delayed version of the Hsync input.<br>(Note: Besides slicing off SOG, the output from this pin gets no other additional processing on the AD9883A. Vsync separation is performed via the sync separator.) |
| <b>SERIAL PORT<br/>(2-Wire)</b> |                                                                                                                                                                                                                                                                                                                                             |
| SDA                             | Serial Port Data I/O                                                                                                                                                                                                                                                                                                                        |
| SCL                             | Serial Port Data Clock                                                                                                                                                                                                                                                                                                                      |
| A0                              | Serial Port Address Input 1<br>For a full description of the 2-wire serial register and how it works, refer to the 2-Wire Serial Control Port section.                                                                                                                                                                                      |

|                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DATA OUTPUTS</b><br>RED<br>GREEN<br>BLUE | Data Output, RED Channel<br>Data Output, GREEN Channel<br>Data Output, BLUE Channel<br>The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATAACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained.                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <b>DATA CLOCK OUTPUTS</b><br>DATAACK        | Data Output Clock<br>This is the main clock output signal used to strobe the output data and HSOUT into external logic. It is produced by the internal clock generator and is synchronous with the internal pixel sampling clock. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATAACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained.                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>INPUTS</b><br>RAIN<br>GAIN<br>BAIN       | Analog Input for RED Channel<br>Analog Input for GREEN Channel<br>Analog Input for BLUE Channel<br>High impedance inputs that accept the RED, GREEN, and BLUE channel graphics signals, respectively. (The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference.) They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.                                                                                                                                                                                                                                                                                                                                                                                                               |
| HSYNC                                       | Horizontal Sync Input<br>This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by serial register 0Eh Bit 6 (Hsync Polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.                                                                                                                                                                                                                                                                                                                        |
| VSYNC                                       | Vertical Sync Input<br>This is the input for vertical sync.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| SOGIN                                       | Sync-on-Green Input<br>This input is provided to assist with processing signals with embedded sync, typically on the GREEN channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 10 mV steps to any voltage between 10 mV and 330 mV above the negative peak of the input signal. The default voltage threshold is 150 mV. When connected to an ac-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal to Hsync.) When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section. |
| CLAMP                                       | External Clamp Input<br>This logic input may be used to define the time during which the input signal is clamped to ground. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting control bit Clamp Function to 1, (register 0FH, Bit 7, default is 0).<br>When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin is controlled by Clamp Polarity register 0FH, Bit 6. When not used, this pin must be grounded and Clamp Function programmed to 0.                                                                                                                                                     |
| COAST                                       | Clock Generator Coast Input (Optional)<br>This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

|                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                | pulses during the vertical interval. The COAST signal is generally <i>not</i> required for PC-generated signals. The logic sense of this pin is controlled by Coast Polarity (register 0FH, Bit 3). When not used, this pin may be grounded and Coast Polarity programmed to 1, or tied HIGH (to VD through a 10 k resistor) and Coast Polarity programmed to 0. Coast Polarity defaults to 1 at power-up.                                                                         |
| REF BYPASS                     | Internal Reference BYPASS<br>Bypass for the internal 1.25 V band gap reference. It should be connected to ground through a 0.1 $\mu$ F capacitor. The absolute accuracy of this reference is $\pm 4\%$ , and the temperature coefficient is $\pm 50$ ppm, which is adequate for most AD9883A applications. If higher accuracy is required, an external reference may be employed instead.                                                                                          |
| MIDSCV                         | Midscale Voltage Reference BYPASS<br>Bypass for the internal midscale voltage reference. It should be connected to ground through a 0.1 $\mu$ F capacitor. The exact voltage varies with the gain setting of the BLUE channel.                                                                                                                                                                                                                                                     |
| FILT                           | External Filter Connection<br>For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.                                                                                                                                                                                                                                              |
| POWER SUPPLY<br>V <sub>D</sub> | Main Power Supply<br>These pins supply power to the main elements of the circuit. They should be as quiet and filtered as possible.                                                                                                                                                                                                                                                                                                                                                |
| V <sub>DD</sub>                | Digital Output Power Supply<br>A large number of output pins (up to 25) switching at high speed (up to 110 MHz) generate a lot of power supply transients (noise). These supply pins are identified separately from the VD pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9883A is interfacing with lower voltage logic, VDD may be connected to a lower supply voltage (as low as 2.5 V) for compatibility. |
| V <sub>D</sub>                 | Clock Generator Power Supply<br>The most sensitive portion of the AD9883A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide "quiet," noise-free power to these pins.                                                                                                                                                                                                      |
| GND                            | Ground<br>The ground return for all circuitry on chip. It is recommended that the AD9883A be assembled on a single solid ground plane, with careful attention to ground current paths.                                                                                                                                                                                                                                                                                             |

## 11.18. MC141585

### 11.18.1. General description

This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto a LCD monitor. Because of the large number of fonts, 512 fonts including 496 standard fonts and 16 multi-color fonts, LMOSD2-16 is suitable to be adopted for the multi-language monitor application especially. It minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision. Programmable hatch pattern generator is added for individual pixel inspection.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. The full OSD menu is formed of 15 rows x 30 columns which can be freely positioned on anywhere of the monitor screen by changing vertical or horizontal delay.

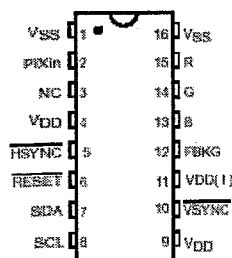
Special functions such as character background color, blinking, bordering or shadowing, four-level windows with programmable size, row double height and double width, programmable vertical height of character and row-to-row spacing, and full-screen erasing and Fade-In/Fade-Out are also incorporated. There are 8 color selections for any individual character display with row intensity attribute and window intensity attribute to expand the color mixture on OSD menu.

### 11.18.2. Features

- Totally 512 Fonts Including 496 Standard Fonts and 16 Multi-Color Fonts.
- 10x18 or 12x18 Font Matrix Selection
- Maximum Pixel CLK of 80MHz
- Maximum input resolution of 1580 dots/line (PIXin/HSYNC ratio)
- Wide Operating Frequency: max. 150KHz for Monitor
- Fully Programmable Character Array of 15 Rows by 30 Columns
- 8-Color Selection for Characters with Color Intensity Attribute on Each Row
- 7-Color Selection for Characters background
- True 16-Color Selection for Windows
- Shadowing on Windows with Programmable Shadow Width/Height/Color
- Fancy Fade-In/Fade-Out Effects
- Programmable Height of Character to Meet Multi-Sync Requirement
- Row To Row Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Character Bordering or Shadowing
- Character/Symbol Blinking Function
- Programmable Vertical and Horizontal Positioning for Display Center
- M\_BUS (IIC) Interface with Address \$7A

### 11.18.3. Pin Description

#### Pin Assignment



#### V<sub>ss</sub>(Pin 1)

This is the ground pin for the chip.

#### PIXin (Pin 2)

This is the Pixel clock input for chip. The MC141585 chip is driven by this pixel clock for all the logics inside.

**NC (Pin 3)**

No connection.

**V<sub>DD</sub> (Pin 4)**

This is the +5V power pin for the chip.

**HSYNC (Pin 5)**

This pin inputs a horizontal synchronize signal. It is negative polarity by default. The leading edge of HSYNC synchronizes its internal horizontal timing. The maximum input ratio between PIXin/HSYNC should not greater than 1580 for displaying 12X18 font matrix. For displaying 10X18 font matrix, this ratio should not greater than 1280.

**RESET (Pin 6)**

An active low signal will reset ROW15 and ROW16 control registers. Refer to Control Registers section for default set-tings. A proper RC network have to be tighten to this pin to ensure the device initialize properly during power up. Refer to the application diagram.

**SDA (Pin 7)**

Data and control message are being transmitted to this chip from a host MCU via M\_bus systems. This wire is configured as a uni-directional data line. (Detailed description of protocols will be discussed in the M\_BUS section).

**SCL (Pin 8)**

A separate synchronizing clock input from the transmitter is required for M\_Bus protocol. Data is read at the rising edge of each clock signal.

**V<sub>DD</sub> (Pin 9)**

This is the power pin for the digital logic of the chip.

**VSYNC (Pin 10)**

Similar to Pin 5, this pin inputs a vertical synchronize signal to synchronize the vertical control circuit. It is negative polarity by default.

**V<sub>DD</sub> (I) (Pin 11)**

This is the voltage supply of RGB outputs when low intensity of Windows/ROW is selected. The RGB output level would be equal to VDD(I) in this case. Please refer to Row Attribute/Window registers for more detail. The input voltage for this pin should be equal to or less than V<sub>DD</sub> (Pin 17) for normal operation.

**FBKG (Pin 12)**

This pin will output a logic high while displaying characters or windows. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

**B,G,R (Pin 13, 14, 15)**

LMOSD2-16 color outputs in CMOS level to the host monitor. These three signals are open drain outputs if 3\_STATE bit is set and the color intensity is inactive. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

**V<sub>ss</sub> (Pin 24)**

This is the ground pin for the digital logic of the chip.

### 11.19. MC34063

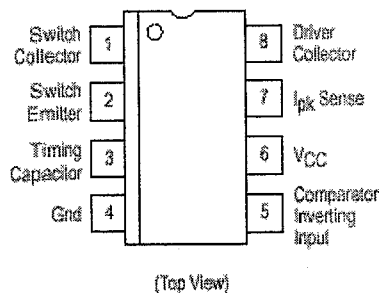
#### 11.19.1. Description

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

#### 11.19.2. Features

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

#### 11.19.3. Pin connections



## 11.20. MSP34X0G

### MSP3400G

#### Multistandard Sound Processor Family

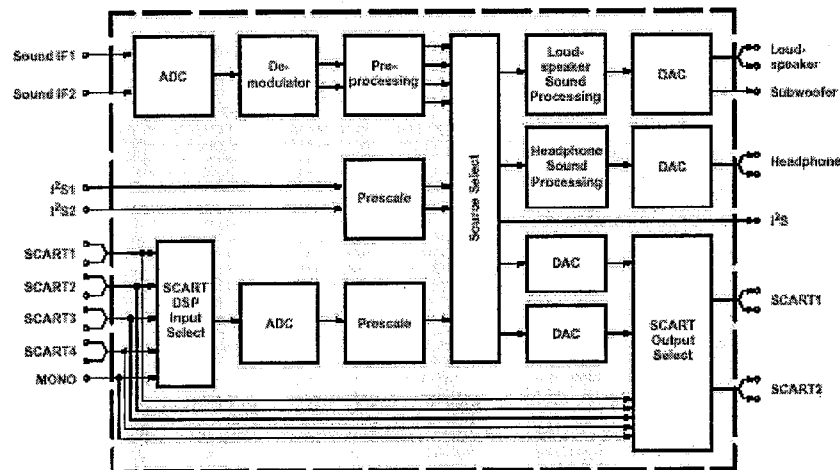
##### 11.20.1. Introduction

The MSP 34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure shows a simplified functional block diagram of the MSP 34x0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard. Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x0G has optimum stereo performance without any adjustments.

All MSP 34x0G versions are pin and software downward compatible to the MSP 34x0D. The MSP 34x0G further simplifies controlling software. Standard selection requires a single I<sup>2</sup>C transmission only.

The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I<sup>2</sup>C interaction is necessary (Automatic Sound Selection).



##### Source Select

I<sup>2</sup>S bus interface consists of five pins:

1. I2S\_DA\_IN1, I2S\_DA\_IN2: For input, four channels (two channels per line, 2\*16 bits) per sampling cycle (32 kHz) are transmitted.
2. I2S\_DA\_OUT: For output, two channels (2\*16 bits) per sampling cycle (32 kHz) are transmitted.
3. I2S\_CL: Gives the timing for the transmission of I<sup>2</sup>S serial data (1.024 MHz).
4. I2S\_WS: The I2S\_WS word strobe line defines the left and right sample.

##### 11.20.2. Features

- Standard Selection with single I<sup>2</sup>C transmission
- Automatic Standard Detection of terrestrial TV standards
- Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS
- Two selectable sound IF (SIF) inputs
- Automatic Carrier Mute function
- Interrupt output programmable (indicating status change)
- Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
- AVC: Automatic Volume Correction
- Subwoofer output with programmable low-pass and complementary high-pass filter

- 5-band graphic equalizer for loudspeaker channel
- Spatial effect for loudspeaker channel
- Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs
- Complete SCART in/out switching matrix
- Two I<sup>2</sup>S inputs; one I<sup>2</sup>S output
- Dolby Pro Logic with DPL 351xA coprocessor
- All analog FM-Stereo A2 and satellite standards; AM-SECAM L standard
- Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM
- Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
- ASTRA Digital Radio (ADR) together with DRP 3510A
- All NICAM standards
- Korean FM-Stereo A2 standard

### 11.20.3. Pin connections

NC = not connected; leave vacant

LV = if not used, leave vacant

OBL = obligatory; connect as described in circuit diagram

DVSS: if not used, connect to DVSS

AHVSS: connect to AHVSS

| Pin No.        |                 |                 |                |                 | Pin Name    | Type   | Connection<br>(if not used) | Short Description                                                            |
|----------------|-----------------|-----------------|----------------|-----------------|-------------|--------|-----------------------------|------------------------------------------------------------------------------|
| PLCC<br>68-pin | PSDIP<br>64-pin | PSDIP<br>52-pin | PQFP<br>80-pin | PLQFP<br>64-pin |             |        |                             |                                                                              |
| 1              | 16              | 14              | 9              | 8               | ADR_WS      | OUT    | LV                          | ADR word strobe                                                              |
| 2              | -               | -               | -              | -               | NC          |        | LV                          | Not connected                                                                |
| 3              | 15              | 13              | 8              | 7               | ADR_DA      | OUT    | LV                          | ADR Data Output                                                              |
| 4              | 14              | 12              | 7              | 6               | I2S_DA_IN1  | IN     | LV                          | I <sup>2</sup> S1 data input                                                 |
| 5              | 13              | 11              | 6              | 5               | I2S_DA_OUT  | OUT    | LV                          | I <sup>2</sup> S data output                                                 |
| 6              | 12              | 10              | 5              | 4               | I2S_WS      | IN/OUT | LV                          | I <sup>2</sup> S word strobe                                                 |
| 7              | 11              | 9               | 4              | 3               | I2S_CL      | IN/OUT | LV                          | I <sup>2</sup> S clock                                                       |
| 8              | 10              | 8               | 3              | 2               | I2C_DA      | IN/OUT | OBL                         | I <sup>2</sup> C data                                                        |
| 9              | 9               | 7               | 2              | 1               | I2C_CL      | IN/OUT | OBL                         | I <sup>2</sup> C clock                                                       |
| 10             | 8               | -               | 1              | 64              | NC          |        | LV                          | Not connected                                                                |
| 11             | 7               | 6               | 80             | 63              | STANDBYQ    | IN     | OBL                         | Stand-by (low-active)                                                        |
| 12             | 6               | 5               | 79             | 62              | ADR_SEL     | IN     | OBL                         | I <sup>2</sup> C bus address select                                          |
| 13             | 5               | 4               | 78             | 61              | D_CTR_I/O_0 | IN/OUT | LV                          | D_CTR I/O_0                                                                  |
| 14             | 4               | 3               | 77             | 60              | D_CTR_I/O_1 | IN/OUT | LV                          | D_CTR I/O_1                                                                  |
| 15             | 3               | -               | 76             | 59              | NC          |        | LV                          | Not connected                                                                |
| 16             | 2               | -               | 75             | 58              | NC          |        | LV                          | Not connected                                                                |
| 17             | -               | -               | -              | -               | NC          |        | LV                          | Not connected                                                                |
| 18             | 1               | 2               | 74             | 57              | AUD_CL_OUT  | OUT    | LV                          | Audio clock output<br>(18.432 MHz)                                           |
| 19             | 64              | 1               | 73             | 56              | TP          |        | LV                          | Test pin                                                                     |
| 20             | 63              | 52              | 72             | 55              | XTAL_OUT    | OUT    | OBL                         | Crystal oscillator                                                           |
| 21             | 62              | 51              | 71             | 54              | XTAL_IN     | IN     | OBL                         | Crystal oscillator                                                           |
| 22             | 61              | 50              | 70             | 53              | TESTEN      | IN     | OBL                         | Test pin                                                                     |
| 23             | 60              | 49              | 69             | 52              | ANA_IN2+    | IN     | AVSS via<br>56 pF/LV        | IF Input 2 (can be left<br>vacant, only if IF input 1 is<br>also not in use) |
| 24             | 59              | 48              | 68             | 51              | ANA_IN-     | IN     | AVSS via<br>56 pF/LV        | IF common (can be left<br>vacant, only if IF input 1 is<br>also not in use)  |
| 25             | 58              | 47              | 67             | 50              | ANA_IN1+    | IN     | LV                          | IF input 1                                                                   |
| 26             | 57              | 46              | 66             | 49              | AVSUP       |        | OBL                         | Analog power supply 5V                                                       |
| -              | -               | -               | 65             | -               | AVSUP       |        | OBL                         | Analog power supply 5V                                                       |
| -              | -               | -               | 64             | -               | NC          |        | LV                          | Not connected                                                                |
| -              | -               | -               | 63             | -               | NC          |        | LV                          | Not connected                                                                |
| 27             | 56              | 45              | 62             | 48              | AVSS        |        | OBL                         | Analog ground                                                                |
| -              | -               | -               | 61             | -               | AVSS        |        | OBL                         | Analog ground                                                                |
| 28             | 55              | 44              | 60             | 47              | MONO_IN     | IN     | LV                          | Mono input                                                                   |
| -              | -               | -               | 59             | -               | NC          |        | LV                          | Not connected                                                                |
| 29             | 54              | 43              | 58             | 46              | VREFTOP     |        | OBL                         | Reference voltage IF A/D<br>converter                                        |
| 30             | 53              | 42              | 57             | 45              | SC1_IN_R    | IN     | LV                          | SCART 1 input, right                                                         |
| 31             | 52              | 41              | 56             | 44              | SC1_IN_L    | IN     | LV                          | SCART 1 input, left                                                          |
| 32             | 51              | -               | 55             | 43              | ASG1        |        | AHVSS                       | Analog Shield Ground 1                                                       |
| 33             | 50              | 40              | 54             | 42              | SC2_IN_R    | IN     | LV                          | SCART 2 input, right                                                         |
| 34             | 49              | 39              | 53             | 41              | SC2_IN_L    | IN     | LV                          | SCART 2 input, left                                                          |
| 35             | 48              | -               | 52             | 40              | ASG2        |        | AHVSS                       | Analog Shield Ground 2                                                       |

|    |    |    |    |    |            |     |             |                              |
|----|----|----|----|----|------------|-----|-------------|------------------------------|
| 36 | 47 | 38 | 51 | 39 | SC3 IN R   | IN  | LV          | SCART 3 input, right         |
| 37 | 46 | 37 | 50 | 38 | SC3 IN L   | IN  | LV          | SCART 3 input, left          |
| 38 | 45 | -  | 49 | 37 | ASG4       |     | AHVSS       | Analog Shield Ground 4       |
| 39 | 44 | -  | 48 | 36 | SC4 IN R   | IN  | LV          | SCART 4 input, right         |
| 40 | 43 | -  | 47 | 35 | SC4 IN L   | IN  | LV          | SCART 4 input, left          |
| 41 | -  | -  | 46 | -  | NC         |     | LV or AHVSS | Not connected                |
| 42 | 42 | 36 | 45 | 34 | AGNDC      |     | OBL         | Analog reference voltage     |
| 43 | 41 | 35 | 44 | 33 | AHVSS      |     | OBL         | Analog ground                |
| -  | -  | -  | 43 | -  | AHVSS      |     | OBL         | Analog ground                |
| -  | -  | -  | 42 | -  | NC         |     | LV          | Not connected                |
| -  | -  | -  | 41 | -  | NC         |     | LV          | Not connected                |
| 44 | 40 | 34 | 40 | 32 | CAPL M     |     | OBL         | Volume capacitor MAIN        |
| 45 | 39 | 33 | 39 | 31 | AHVSUP     |     | OBL         | Analog power supply 8V       |
| 46 | 38 | 32 | 38 | 30 | CAPL A     |     | OBL         | Volume capacitor AUX         |
| 47 | 37 | 31 | 37 | 29 | SC1 OUT L  | OUT | LV          | SCART output 1, left         |
| 48 | 36 | 30 | 36 | 28 | SC1 OUT R  | OUT | LV          | SCART output 1, right        |
| 49 | 35 | 29 | 35 | 27 | VREF1      |     | OBL         | Reference ground 1           |
| 50 | 34 | 28 | 34 | 26 | SC2 OUT L  | OUT | LV          | SCART output 2, left         |
| 51 | 33 | 27 | 33 | 25 | SC2 OUT R  | OUT | LV          | SCART output 2, right        |
| 52 | -  | -  | 32 | -  | NC         |     | LV          | Not connected                |
| 53 | 32 | -  | 31 | 24 | NC         |     | LV          | Not connected                |
| 54 | 31 | 26 | 30 | 23 | DACM SUB   | OUT | LV          | Subwoofer output             |
| 55 | 30 | -  | 29 | 22 | NC         |     | LV          | Not connected                |
| 56 | 29 | 25 | 28 | 21 | DACM L     | OUT | LV          | Loudspeaker out, left        |
| 57 | 28 | 24 | 27 | 20 | DACM R     | OUT | LV          | Loudspeaker out, right       |
| 58 | 27 | 23 | 26 | 19 | VREF2      |     | OBL         | Reference ground 2           |
| 59 | 26 | 22 | 25 | 18 | DACA L     | OUT | LV          | Headphone out, left          |
| 60 | 25 | 21 | 24 | 17 | DACA R     | OUT | LV          | Headphone out, right         |
| -  | -  | -  | 23 | -  | NC         |     | LV          | Not connected                |
| -  | -  | -  | 22 | -  | NC         |     | LV          | Not connected                |
| 61 | 24 | 20 | 21 | 16 | RESETQ     | IN  | OBL         | Power-on-reset               |
| 62 | 23 | -  | 20 | 15 | NC         |     | LV          | Not connected                |
| 63 | 22 | -  | 19 | 14 | NC         |     | LV          | Not connected                |
| 64 | 21 | 19 | 18 | 13 | NC         |     | LV          | Not connected                |
| 65 | 20 | 18 | 17 | 12 | I2S_DA_IN2 | IN  | LV          | I <sup>2</sup> S2-data input |
| 66 | 19 | 17 | 16 | 11 | DVSS       |     | OBL         | Digital ground               |
| -  | -  | -  | 15 | -  | DVSS       |     | OBL         | Digital ground               |
| -  | -  | -  | 14 | -  | DVSS       |     | OBL         | Digital ground               |
| 67 | 18 | 16 | 13 | 10 | DVSUP      |     | OBL         | Digital power supply 5V      |
| -  | -  | -  | 12 | -  | DVSUP      |     | OBL         | Digital power supply 5V      |
| -  | -  | -  | 11 | -  | DVSUP      |     | OBL         | Digital power supply 5V      |
| 68 | 17 | 15 | 10 | 9  | ADR_CL     | OUT | LV          | ADR clock                    |

## 12. SERVICE MENU SETTINGS

All system, geometry and white balance alignments are performed in production service mode. Before starting the production mode alignments, make sure that all manual adjustments are done correctly. To start production mode alignments enter the main menu by pressing "M" button and then press the digits 4, 7, 2 and 5 buttons respectively. The following menu appears on the screen.

| Service                                   |
|-------------------------------------------|
| ▶ Adjust...<br>Options...<br>Aps Wss Test |
| TFT20 Version Time Date                   |

After entering the Service menu, you can access its items by pressing "▲/▼" buttons. In order to enter selected menu, use "◀/▶" buttons. To exit the service menu press "M" button. Entire service menu parameters of TFT TV are listed below.

### 12.1. ADJUST MENU SETTINGS

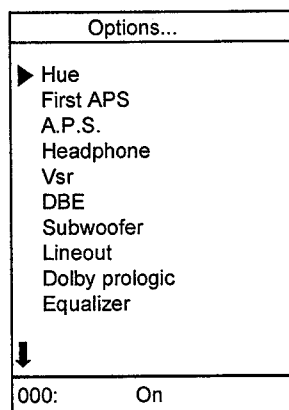
In order to enter Adjust menu, move the cursor to Adjust... parameter by pressing "▲/▼" buttons in Service Menu and press "◀/▶" button. The following menu appears on the screen.

| Adjust...            |
|----------------------|
|                      |
| P 08 CNN S 04 BG 463 |

There is no items for adjustment in ADJUST menu for now.

## 12.2. OPTIONS MENU SETTINGS

In order to enter Options menu, move the cursor to **Options...** parameter by pressing "**▲/▼**" buttons in Service Menu and press "**◀/▶**" button. The following menu appears on the screen.



There are 50 items in the OPTIONS menu, but 10 of them are seen when you first enter the menu. Using "**▲/▼**" buttons remaining items can be seen.

**Hue** **On/Off**  
Set ON

**First APS** **On/Off**  
If ON, TV starts with APS menu at Start-up. Set OFF

**A.P.S** **On/Off**  
enable/disable Automatic Programming System. Set ON

**Headphone** **On/Off**  
enable/disable the usage of the HP and HP related items in sound menu. Set ON

**Vsr** **On/Off**  
enable/disable Vsr. Set OFF

**DBE** **On/Off**  
enable/disable DBE. Set OFF

**Subwoofer** **On/Off**  
enable/disable Subwoofer. Set OFF

**Lineout** **On/Off**  
enable/disable Lineout. Set ON

**Dolby prologic** **On/Off**  
enable/disable dolby prologic system. Set OFF

**Equalizer** **On/Off**  
enable/disable equalizer system. Set ON

**BG** **On/Off**  
enable/disable BG Standard. Set ON

**DK** **On/Off**  
enable/disable DK Standard. Set OFF

| Options... |               |
|------------|---------------|
| ↑          |               |
|            | Equalizer     |
|            | BG            |
|            | DK            |
|            | I             |
|            | L             |
|            | L'            |
|            | M             |
|            | N             |
|            | NM            |
| ▶          | FM Prs Avl On |
| ↓          |               |
| 018:       | Off           |

**I** On/Off  
enable/disable I Standard. Set OFF

**L** On/Off  
enable/disable L Standard. Set OFF

**L'** On/Off  
enable/disable L' Standard. Set OFF

**M** On/Off  
enable/disable M Standard. Set OFF

**N** On/Off  
enable/disable N Standard. Set OFF

**NM** On/Off  
enable/disable NM Standard. Set OFF

#### FM Prs Avl On

Adjusts the FM Prescaler value, when Automatic Volume Levelling is On

Min. Value: 0000 00000

Max. Value: 00FF 00255

Recommended Value: 000F 00015: for 16 ohm

| Options... |                      |
|------------|----------------------|
| ↑          |                      |
|            | FM Prs Avl On        |
|            | Nicam Prs Avl On     |
|            | Scart Prs Avl On     |
|            | Scart Volume Avl On  |
|            | FM Prs Avl Off       |
|            | Nicam Prs Avl Off    |
|            | Scart Prs Avl Off    |
|            | Scart Volume Avl Off |
|            | X                    |
| ▶          | X                    |
| ↓          |                      |
| 027:       | FFFF 65535 ◀▶        |

**Nicam Prs Avl On**

Adjusts the Nicam Prescaler value, when Automatic Volume Levelling is On

|                    |      |                   |
|--------------------|------|-------------------|
| Min. Value:        | 0000 | 00000             |
| Max. Value:        | 00FF | 00255             |
| Recommended Value: | 0022 | 00035: for 16 ohm |

**Scart Prs Avl On**

Adjusts the Scart Prescaler value, when Automatic Volume Levelling is On

|                    |      |                   |
|--------------------|------|-------------------|
| Min. Value:        | 0000 | 00000             |
| Max. Value:        | 00FF | 00255             |
| Recommended Value: | 000F | 00015: for 16 ohm |

**Scart Volume Avl On**

Adjusts the Scart Volume value, when Automatic Volume Levelling is On

|                    |      |                   |
|--------------------|------|-------------------|
| Min. Value:        | 0000 | 00000             |
| Max. Value:        | 00FF | 00255             |
| Recommended Value: | 0035 | 00051: for 16 ohm |

**FM Prs Avl Off**

Adjusts the FM Prescaler value, when Automatic Volume Levelling is Off

|                    |      |                   |
|--------------------|------|-------------------|
| Min. Value:        | 0000 | 00000             |
| Max. Value:        | 00FF | 00255             |
| Recommended Value: | 0008 | 00012: for 16 ohm |

**Nicam Prs Avl Off**

Adjusts the Nicam Prescaler value, when Automatic Volume Levelling is Off

|                    |      |                   |
|--------------------|------|-------------------|
| Min. Value:        | 0000 | 00000             |
| Max. Value:        | 00FF | 00255             |
| Recommended Value: | 0013 | 00028: for 16 ohm |

**Scart Prs Avl Off**

Adjusts the Scart Prescaler value, when Automatic Volume Levelling is Off

|                    |      |                   |
|--------------------|------|-------------------|
| Min. Value:        | 0000 | 00000             |
| Max. Value:        | 00FF | 00255             |
| Recommended Value: | 0008 | 00012: for 16 ohm |

**Scart Volume Avl Off**

Adjusts the Scart Volume value, when Automatic Volume Levelling is Off

|                    |      |                   |
|--------------------|------|-------------------|
| Min. Value:        | 0000 | 00000             |
| Max. Value:        | 00FF | 00255             |
| Recommended Value: | 0035 | 00051: for 16 ohm |

**X**

Not used

| Options... |          |
|------------|----------|
| ↑          |          |
|            | X        |
|            | X        |
|            | X        |
|            | Avl      |
|            | Top TXT  |
|            | Fast TXT |
|            | TXT Lang |
|            | IF Freq  |
|            | Sound    |
| ▶          | Carrier  |
| ↓          |          |
| 036:       | On       |

**Avi** **On/Off**  
enable/disable Automatic Volume Levelling System. Set **ON**

**Top TXT** **On/Off**  
enable/disable TopText. Set **OFF**

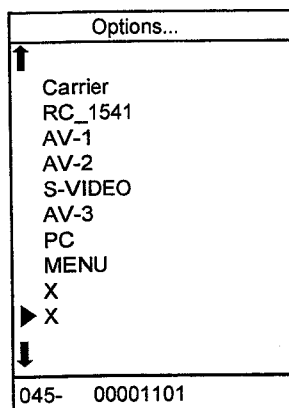
**Fast TXT** **On/Off**  
enable/disable FastText. Set **ON**

**TXT Lang**  
Switches between Teletext Language Groups  
Min. Value: 0000 00000  
Max. Value: 0004 00004  
Recommended Value: 0000 00000

**IF Freq**  
Adjusts the IF Frequency  
Min. Value: 0000 00000  
Max. Value: 00FF 00255  
Recommended Value: 0000 00000

**Sound** **On/Off**  
enable/disable Sound. Set **ON**

**Carrier** **On/Off**  
enable/disable Carrier. Set **ON**



**RC\_1541** **On/Off**  
Enables/disables Remote control usage for Service menu. Set **ON**.

**AV-1** **On/Off**  
enable/disable AV-1. Set **ON**

**AV-2** **On/Off**  
enable/disable AV-2. Set **ON**

**S-VIDEO** **On/Off**  
enable/disable S-VIDEO. Set **ON**

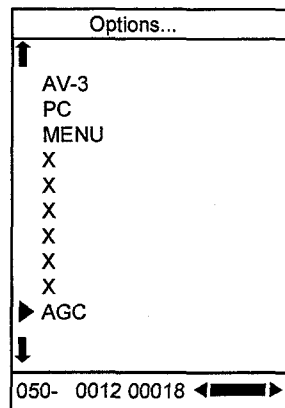
**AV-3** **On/Off**  
enable/disable AV-3. Set **ON**

**PC** **On/Off**  
enable/disable PC. Set **ON**

**MENU** **On/Off**  
enable/disable semi-transparent MENU. Set OFF.

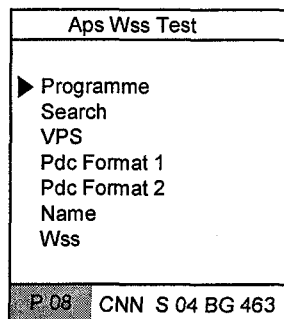
**X**  
Not used.

**AGC**  
Adjusts the Automatic Gain Control value.  
Min. Value: 0000 00000  
Max. Value: 001F 00031  
Recommended Value: 000A 00010



### 12.3. APS WSS TEST MENU

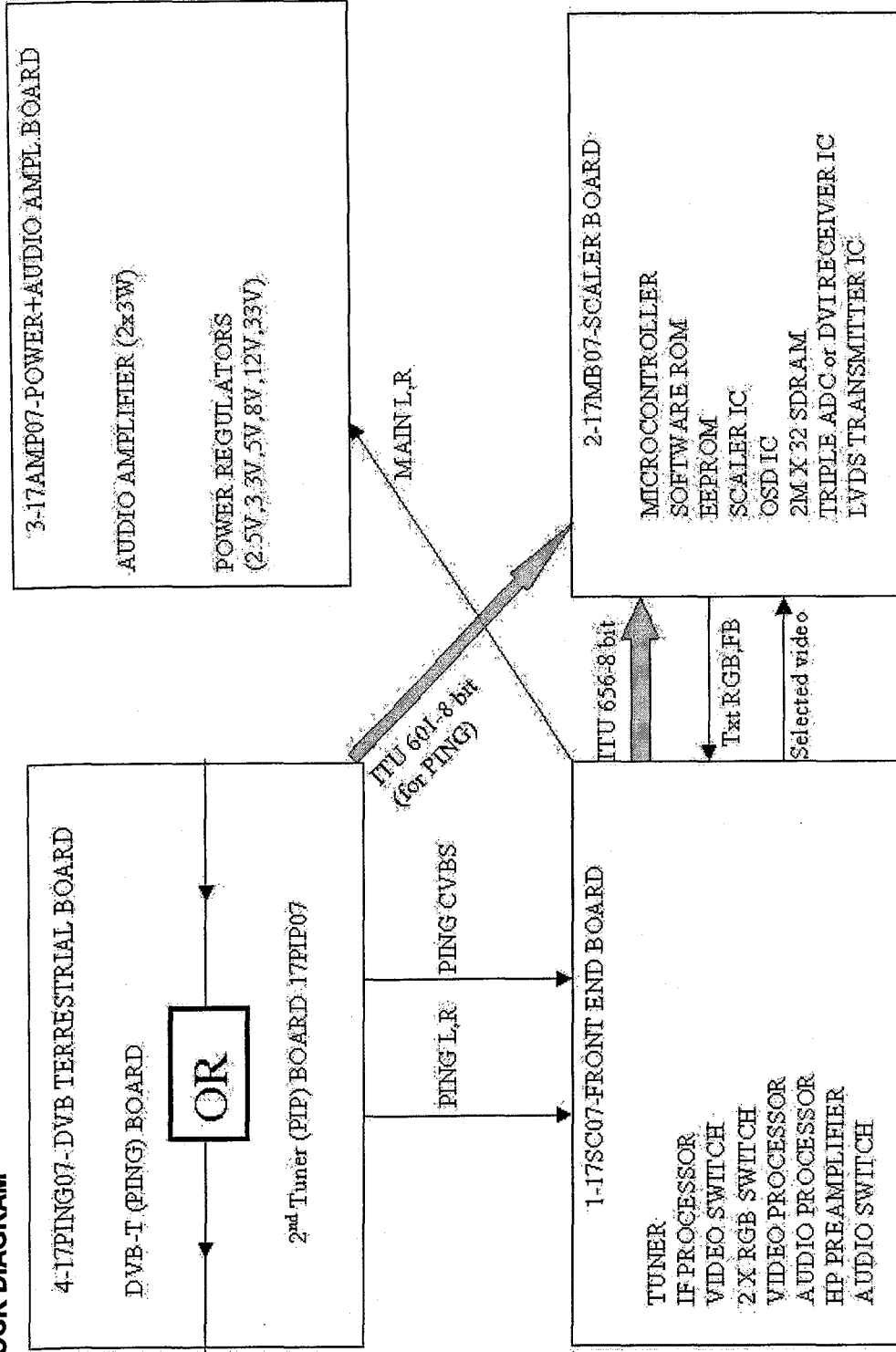
In order to enter Aps Wss Test menu, move the cursor to **Aps Wss Test** parameter by pressing "▲/▼" buttons in Service Menu and press "◀/▶" button. The following menu appears on the screen.

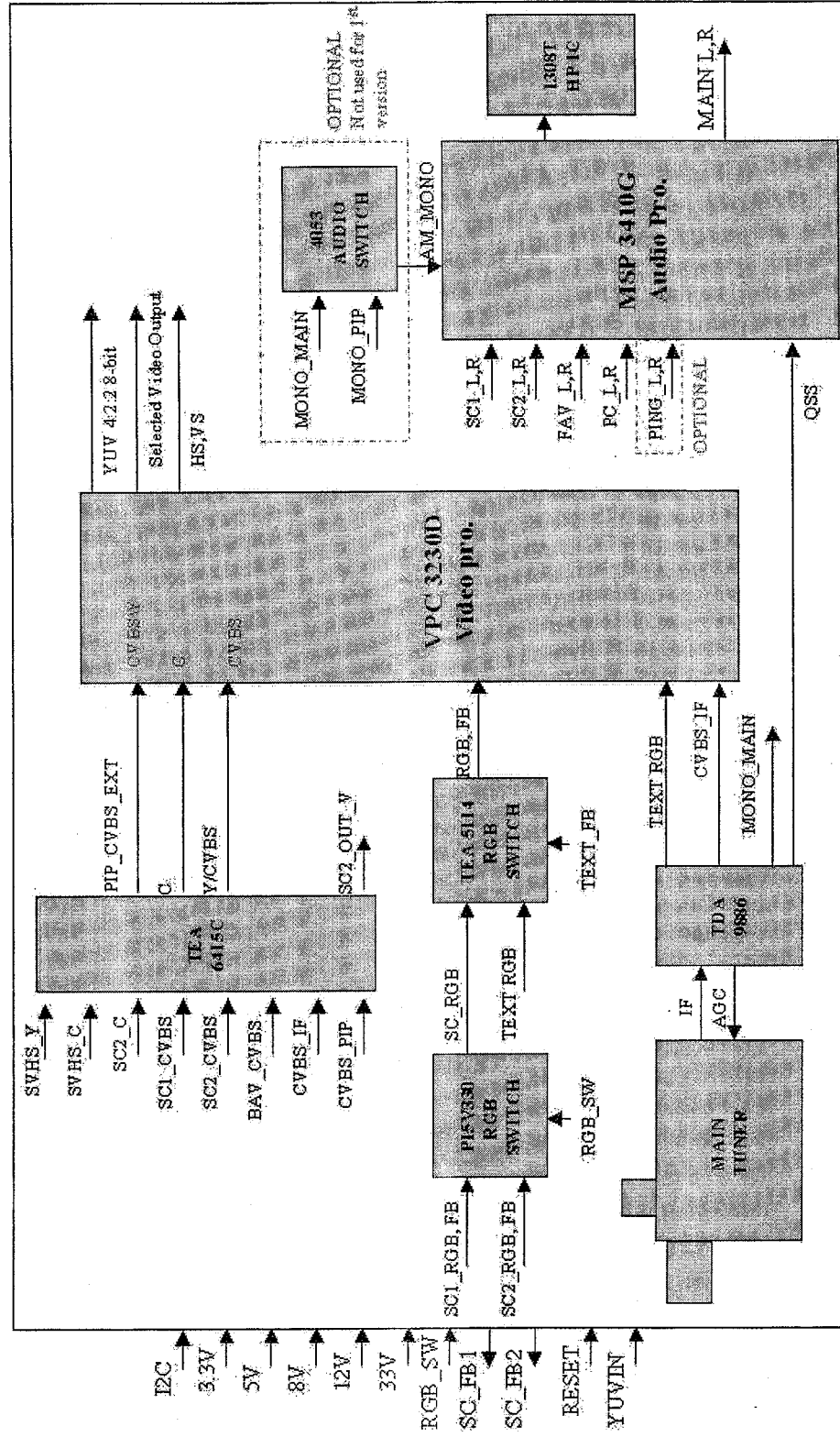


There are 7 items in the Aps Wss Test menu.

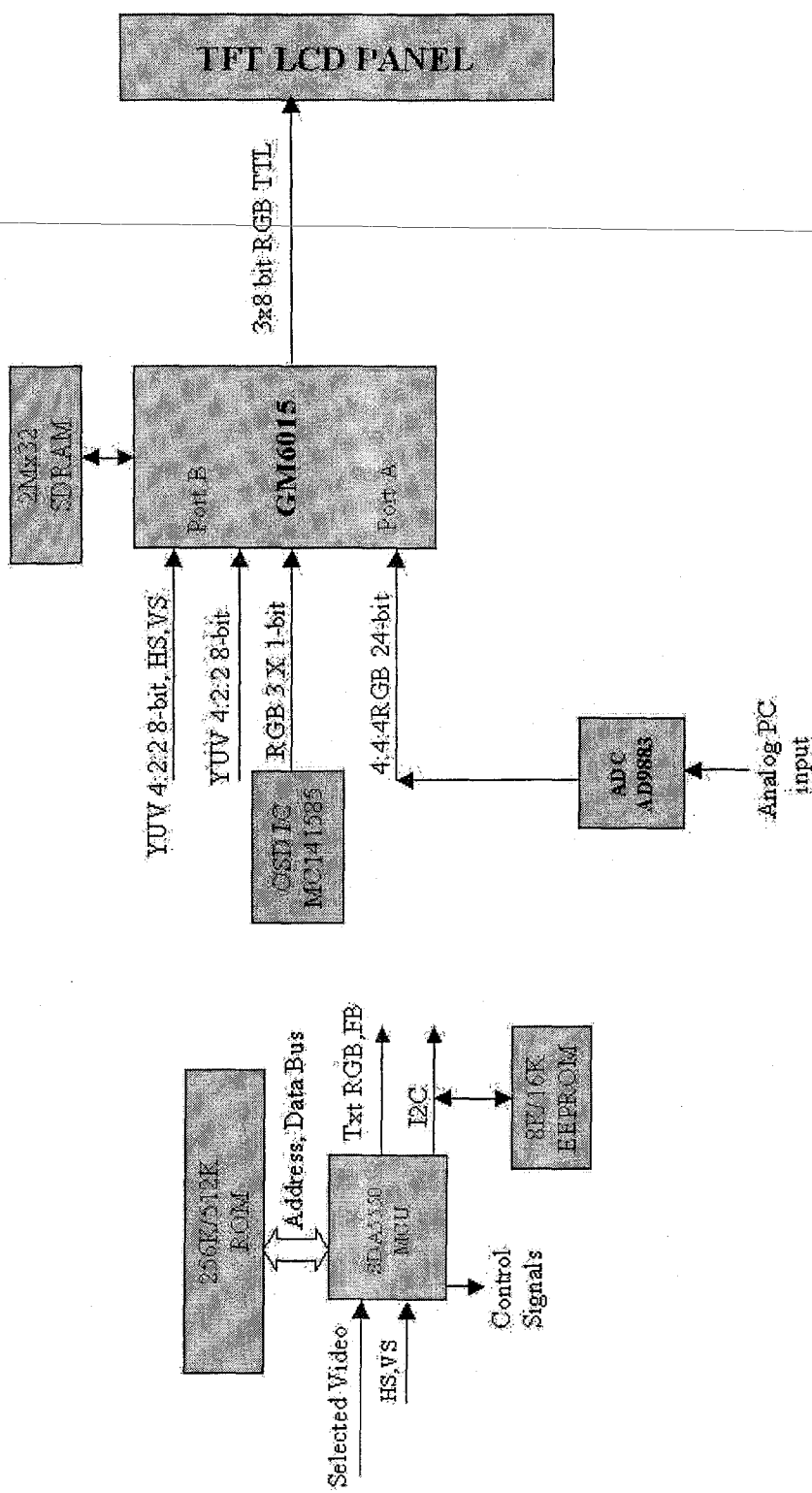
Programme  
Search  
VPS  
Pdc Format 1  
Pdc Format 2  
Name  
Wss

### 13. BLOCK DIAGRAM

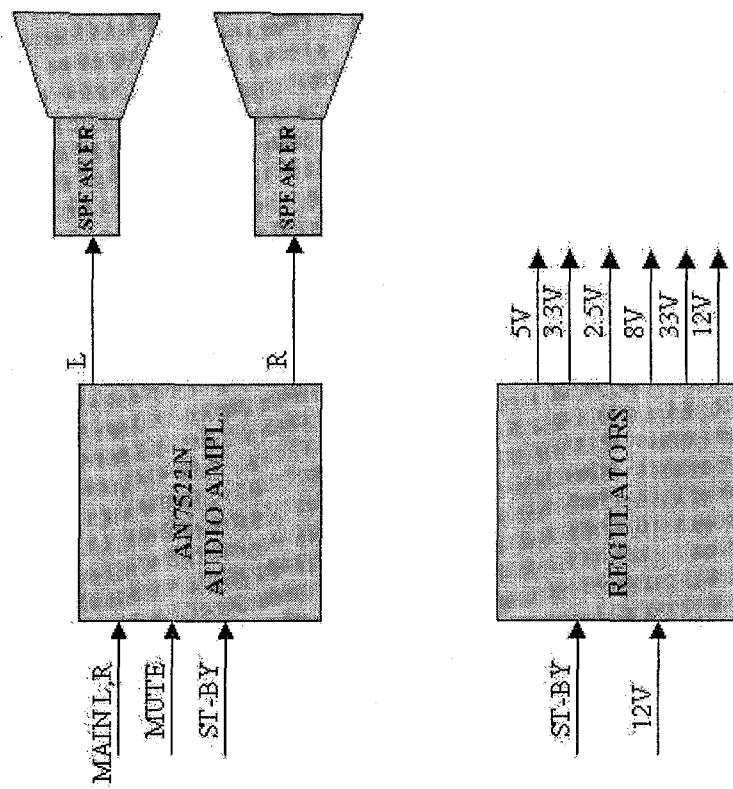




FRONT END BOARD

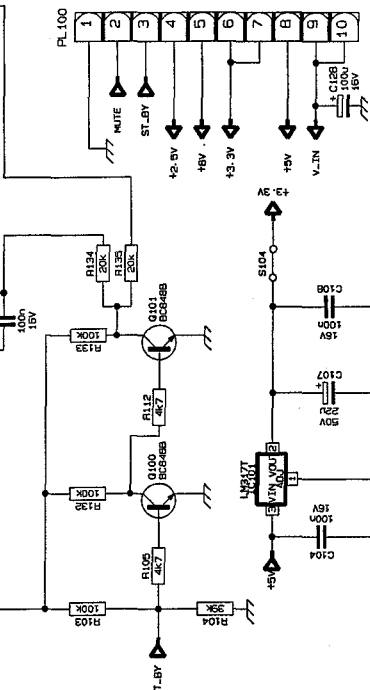
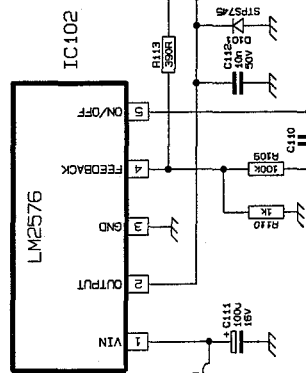
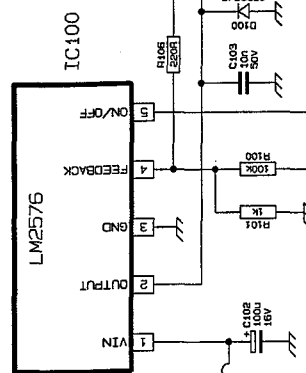


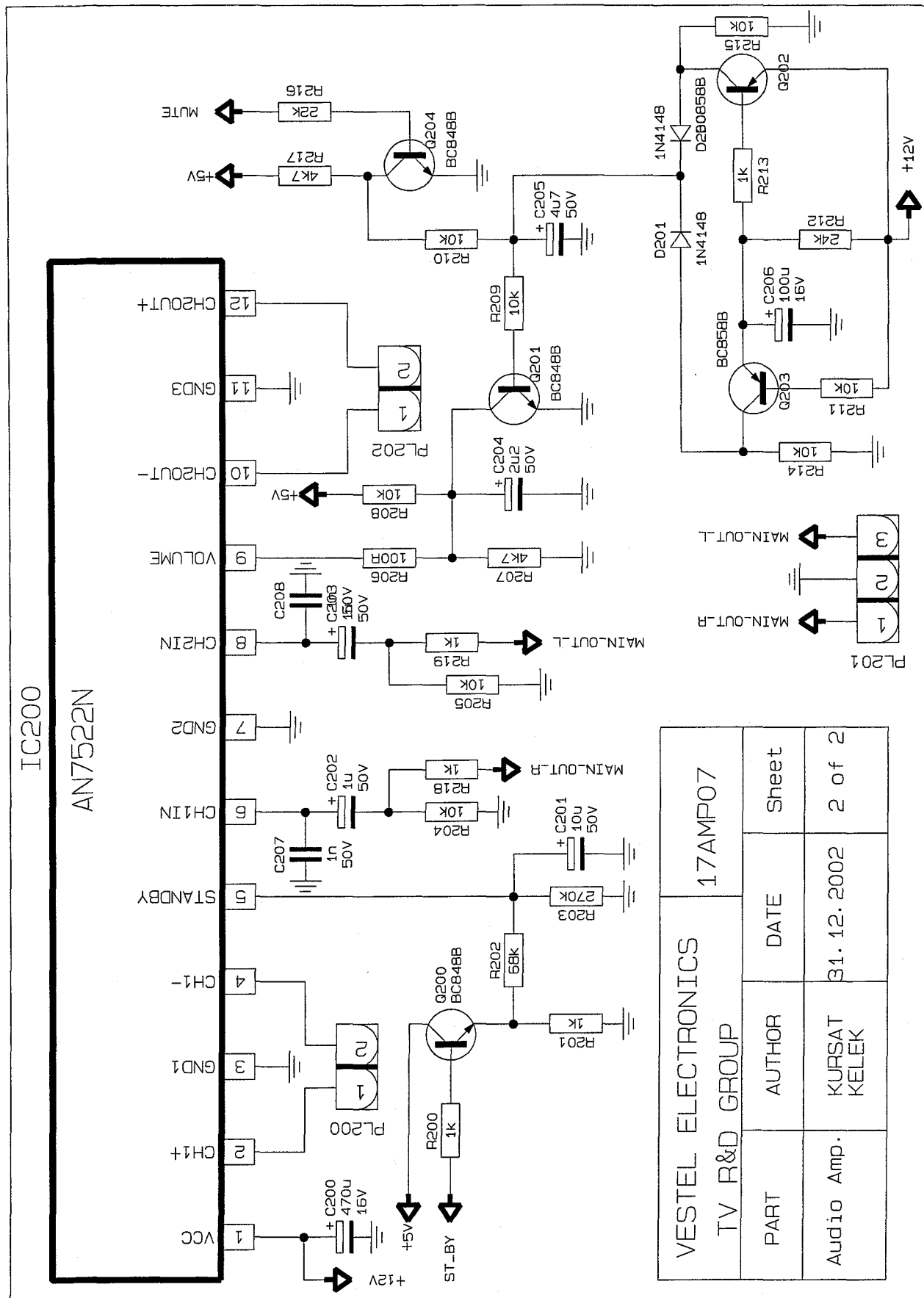
SCALER BOARD

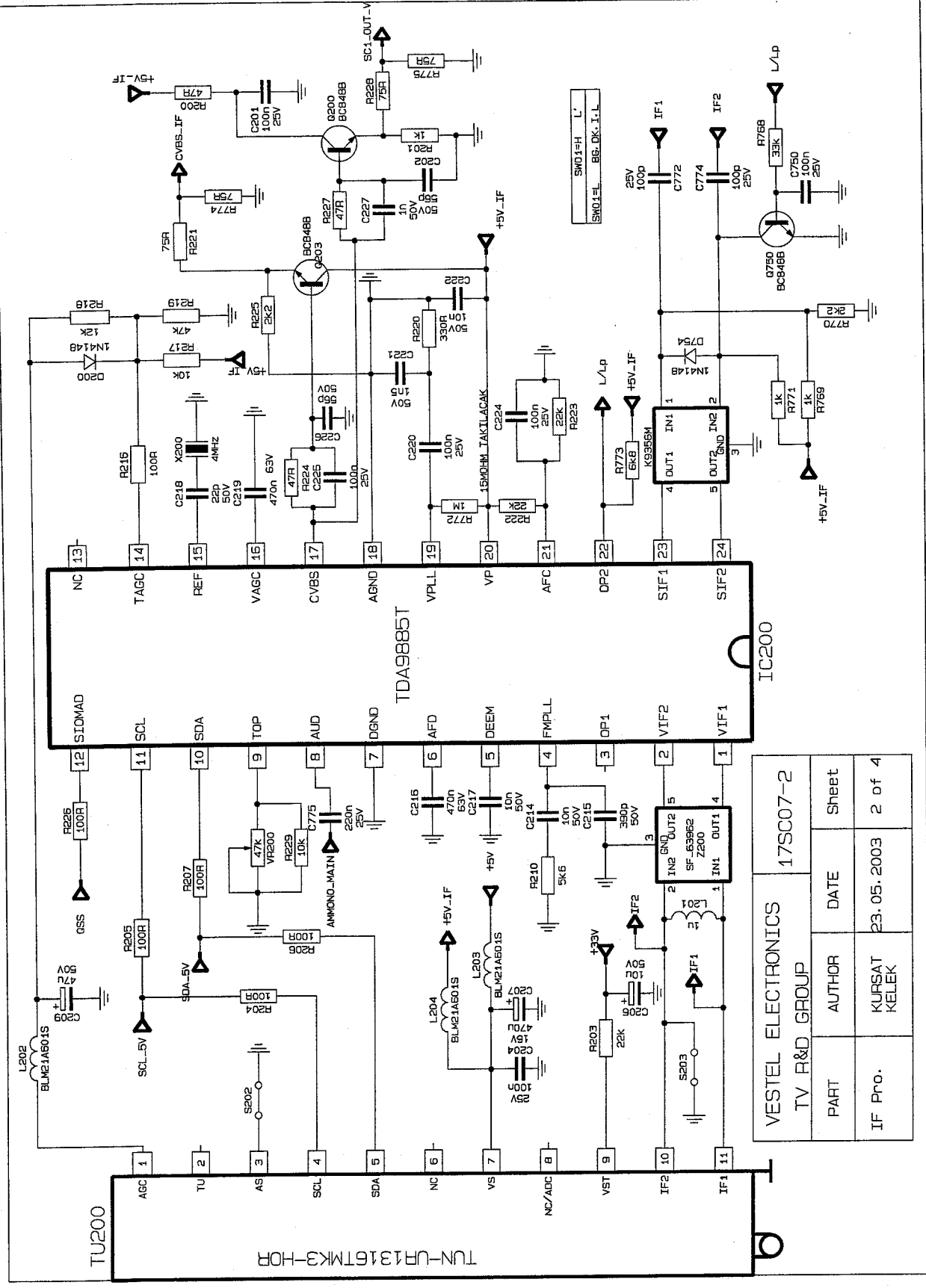


POWER+AUDIO AMP. BOARD

| PART       | AUTHOR       | DATE       | Sheet  |
|------------|--------------|------------|--------|
| Power Reg. | KURSAT KELEK | 31.12.2002 | 1 of 2 |

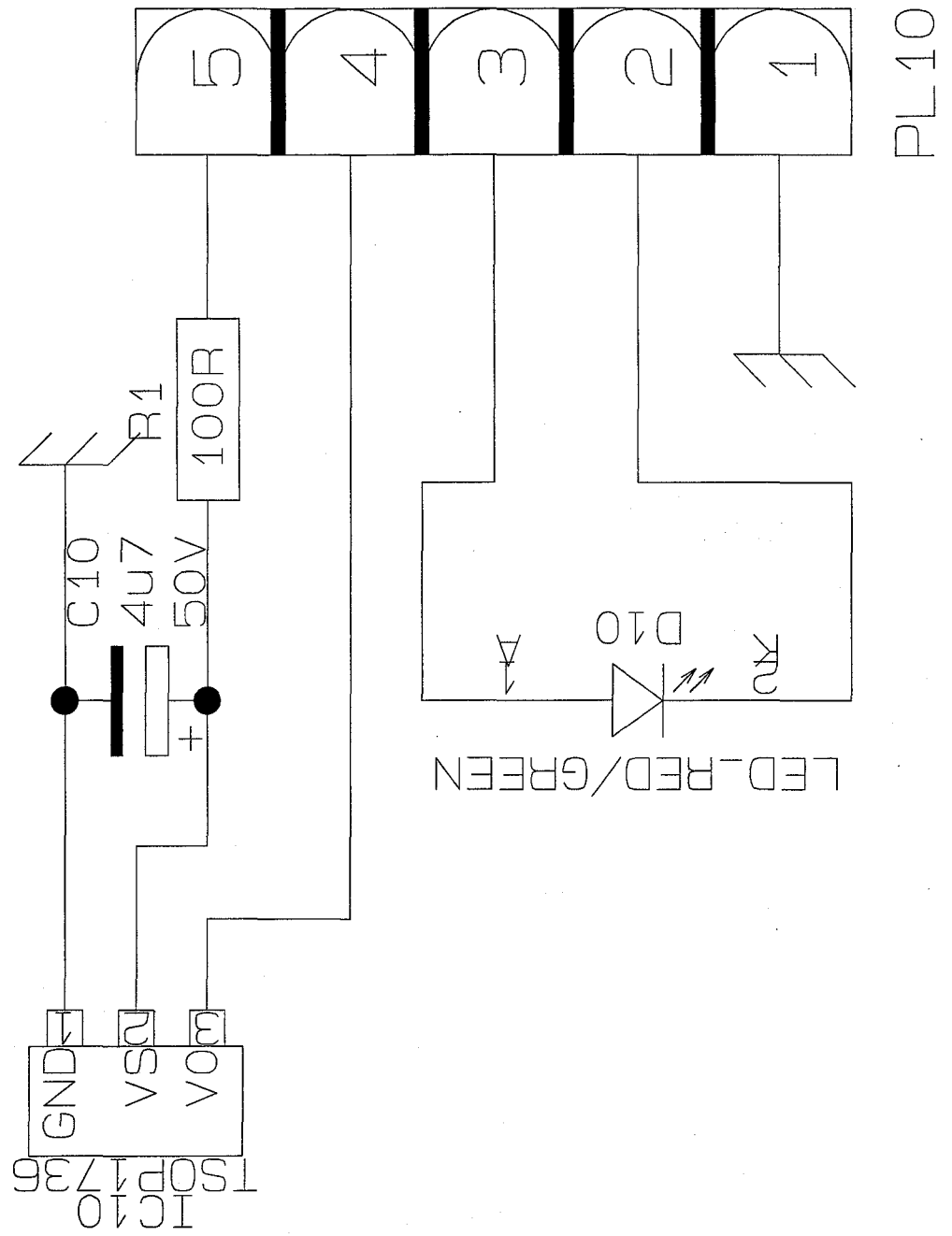


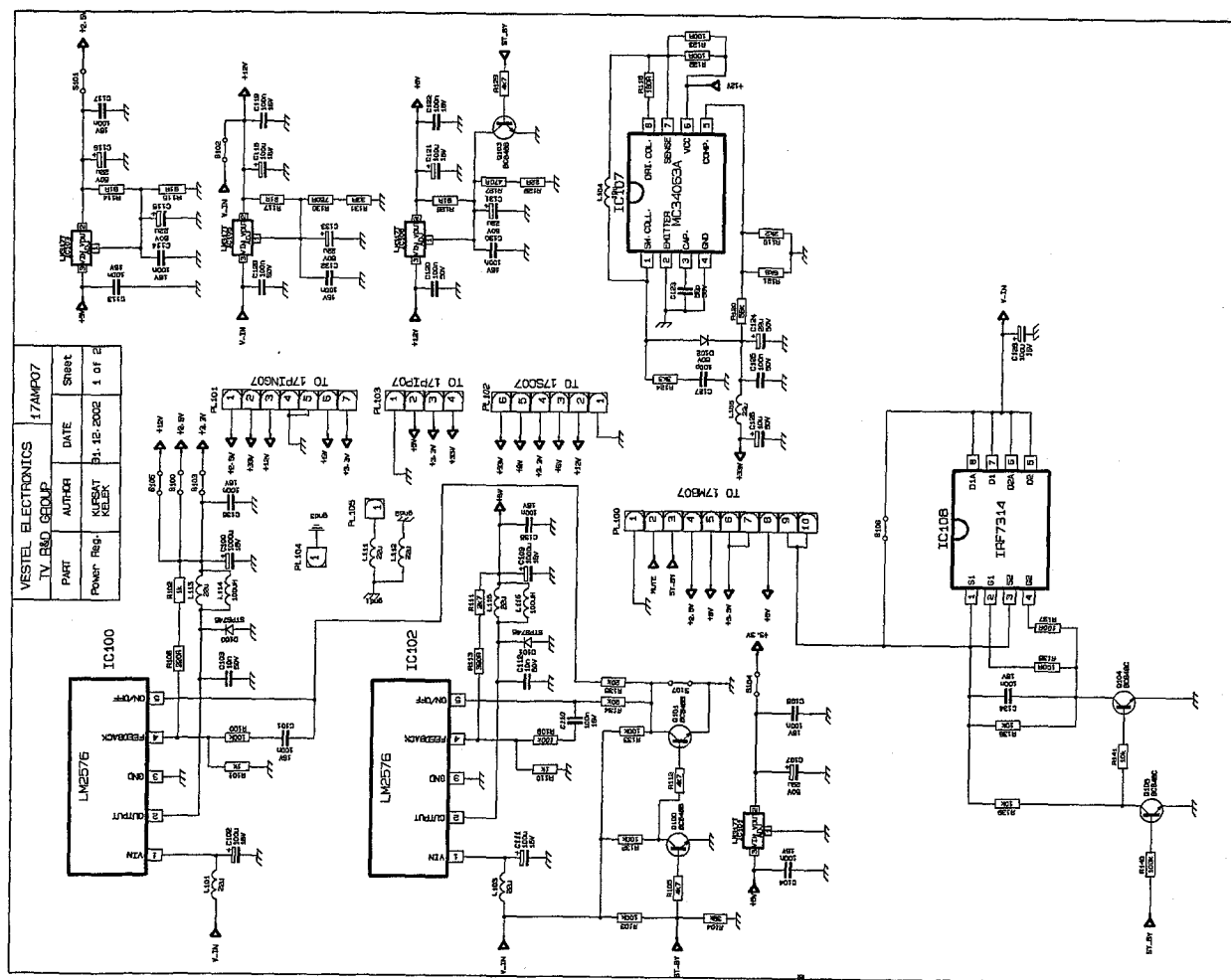


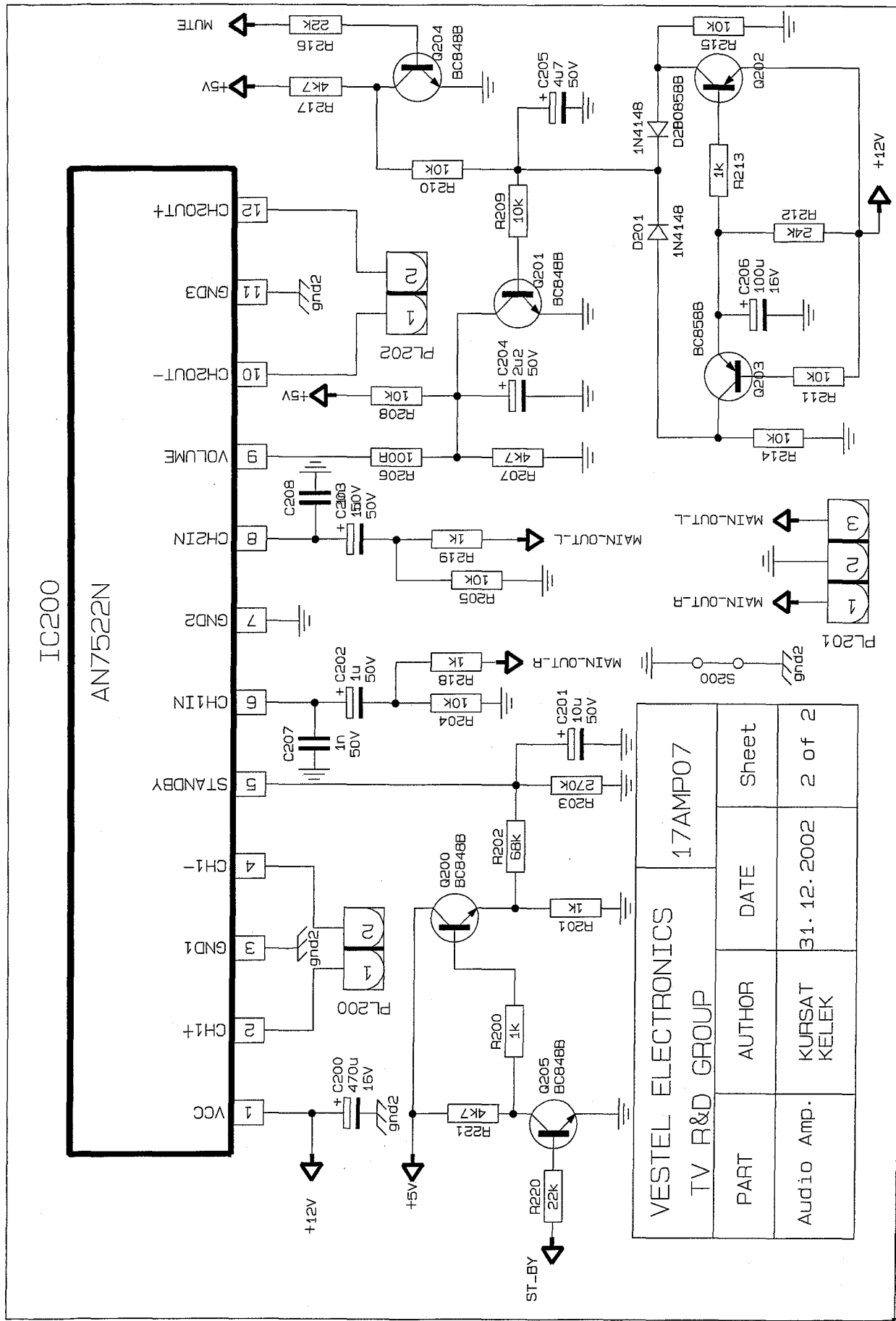


|                    |              |            |        |
|--------------------|--------------|------------|--------|
| VESTEL ELECTRONICS |              | 17SC07-2   |        |
| TV R&D GROUP       |              | Sheet      |        |
| PART               | AUTHOR       | DATE       | 2 of 4 |
| IF Pro.            | KURSAT KELEK | 23.05.2003 |        |

A









A

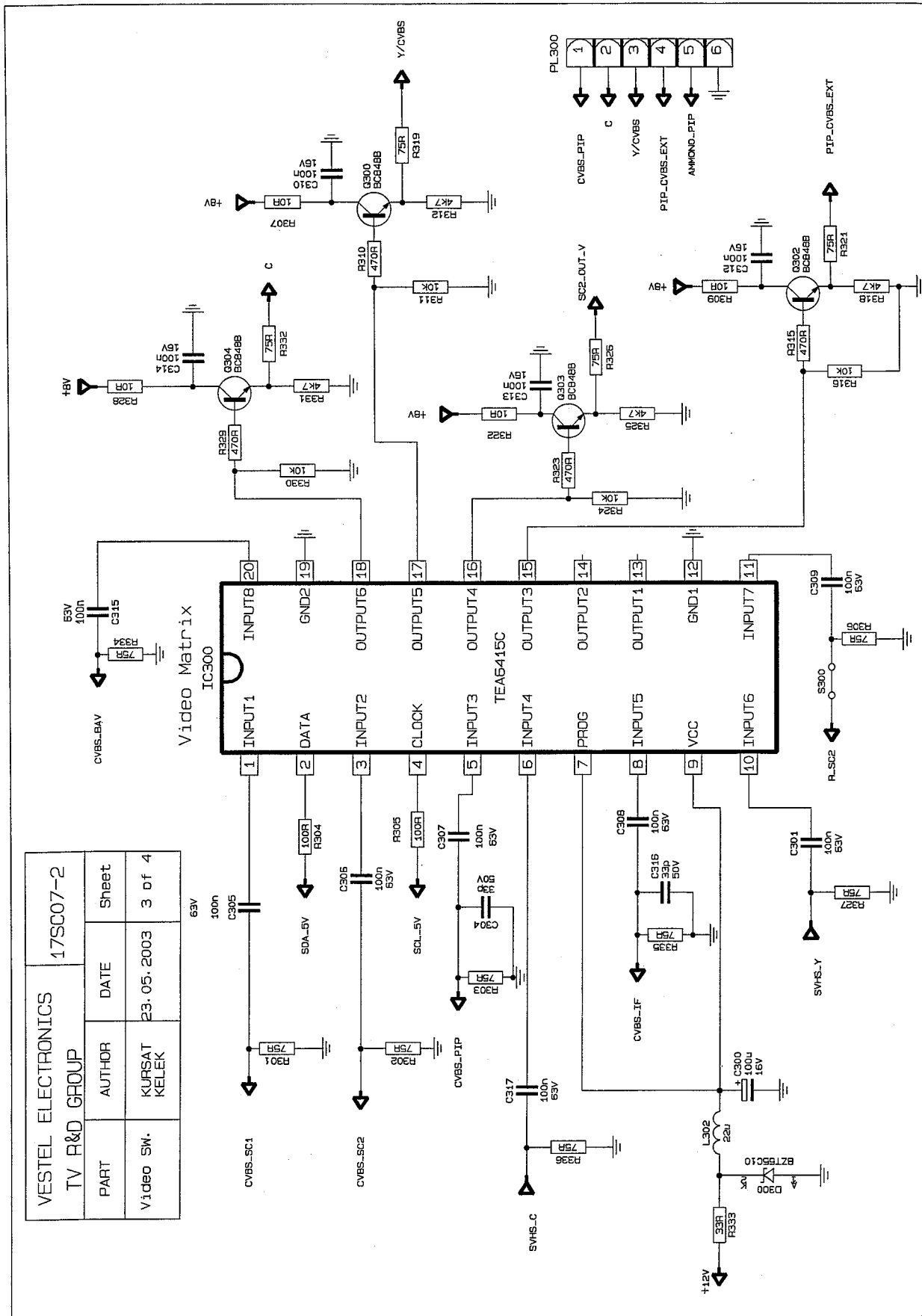
B

C

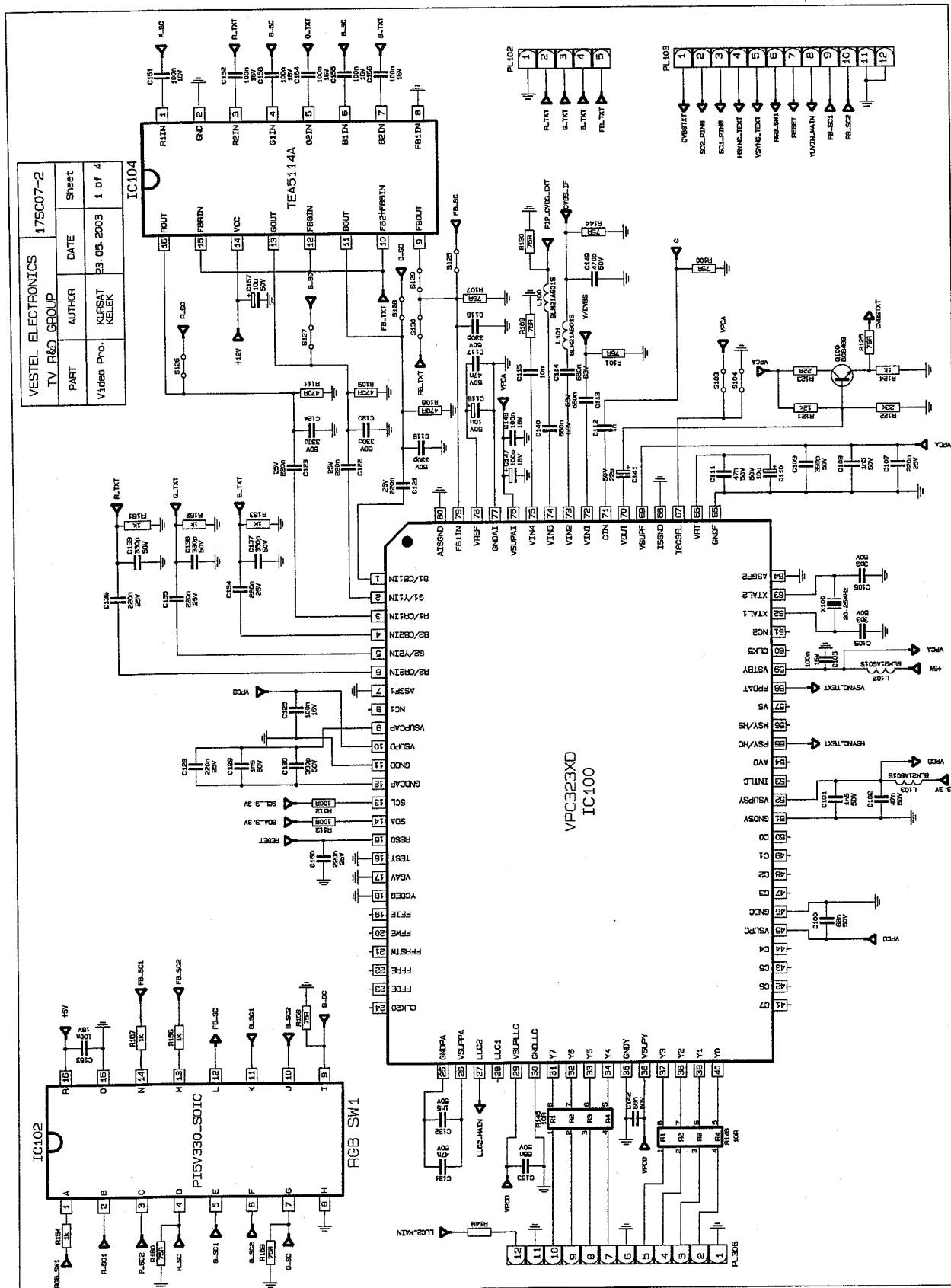
D

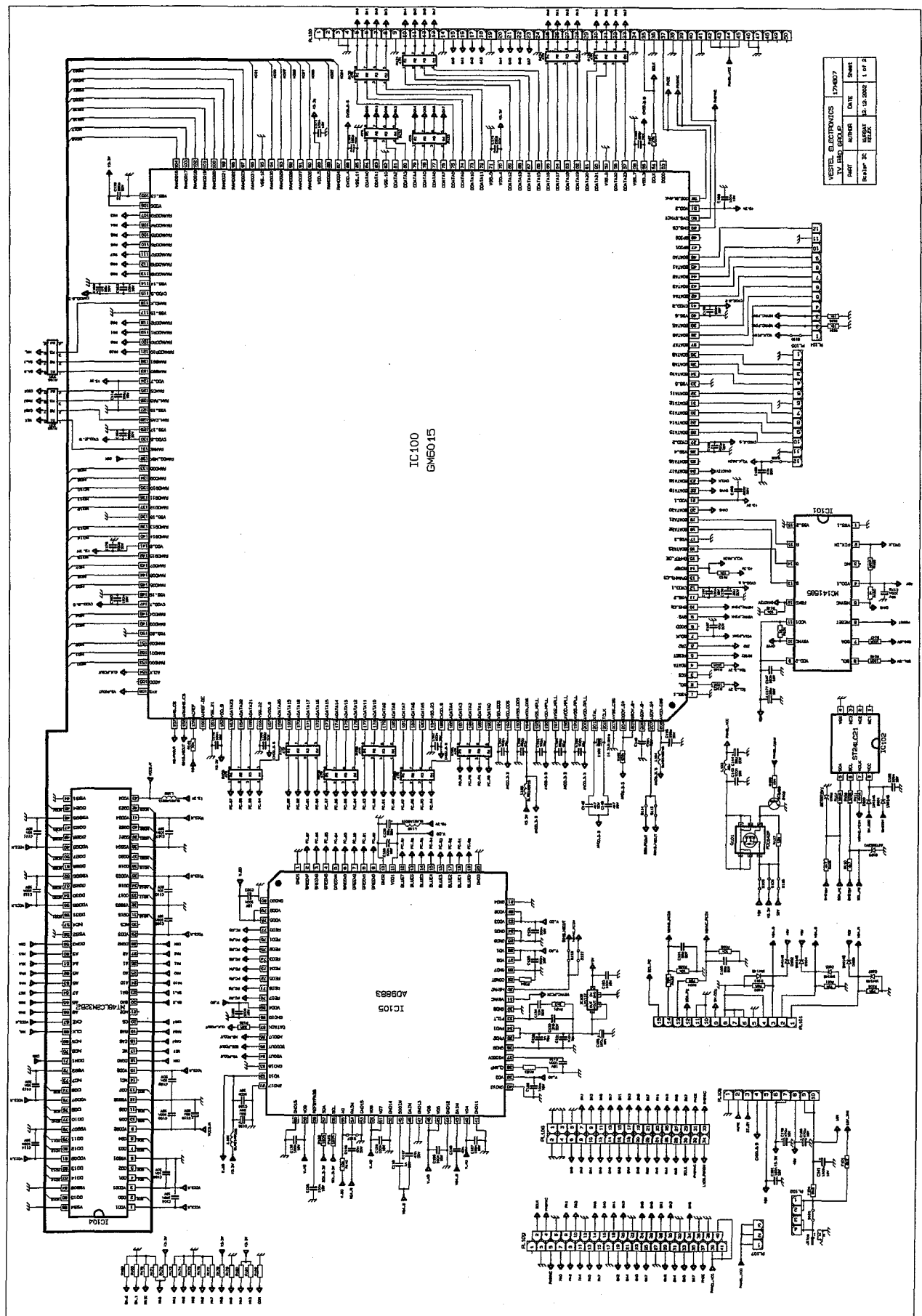
E

|                    |              |            |        |
|--------------------|--------------|------------|--------|
| VESTEL ELECTRONICS |              | 17SC07-2   |        |
| TV R&D GROUP       |              | Sheet      |        |
| PART               | AUTHOR       | DATE       | 3 of 4 |
| Video SW.          | KURSAT KELEK | 23.05.2003 |        |

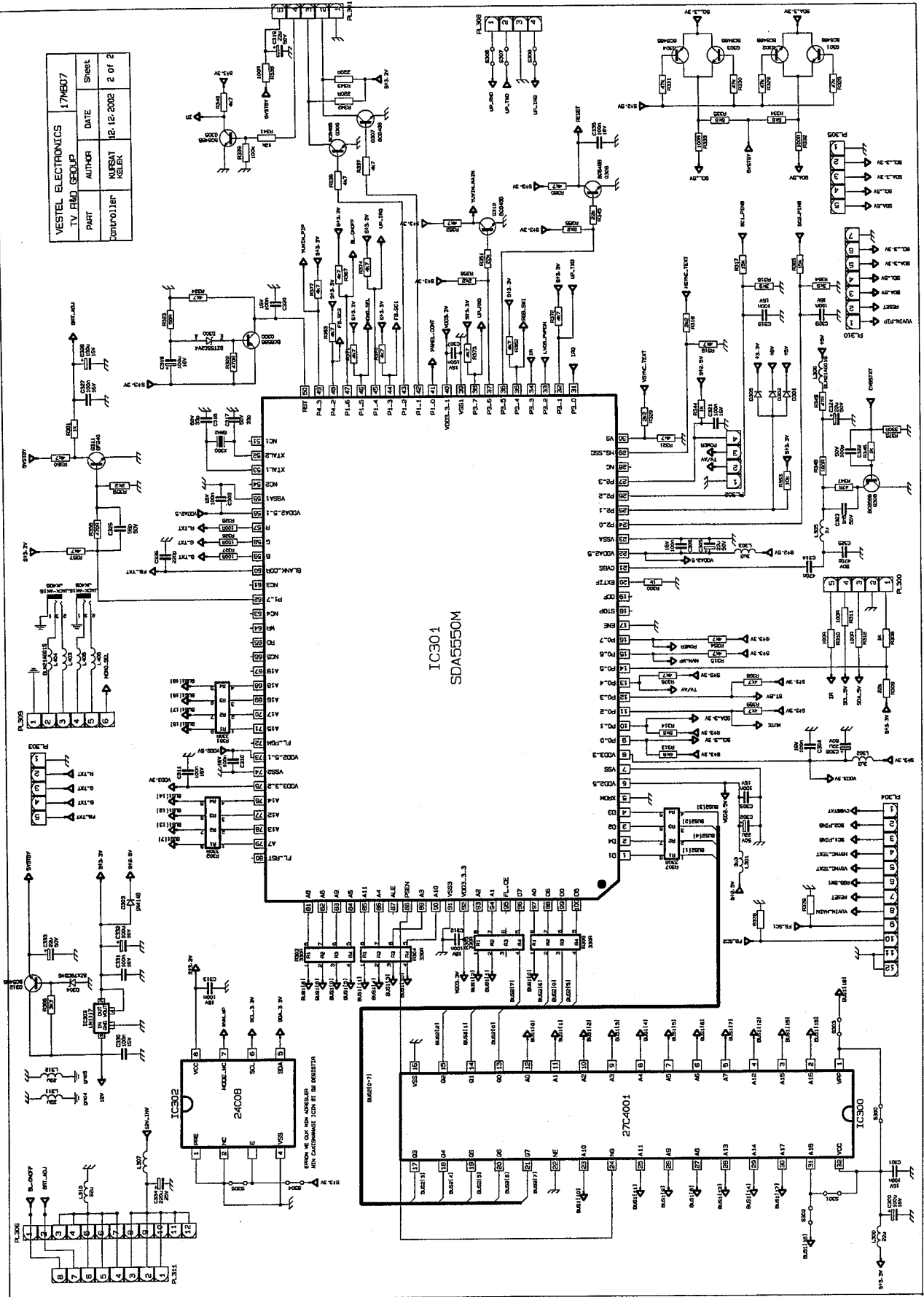


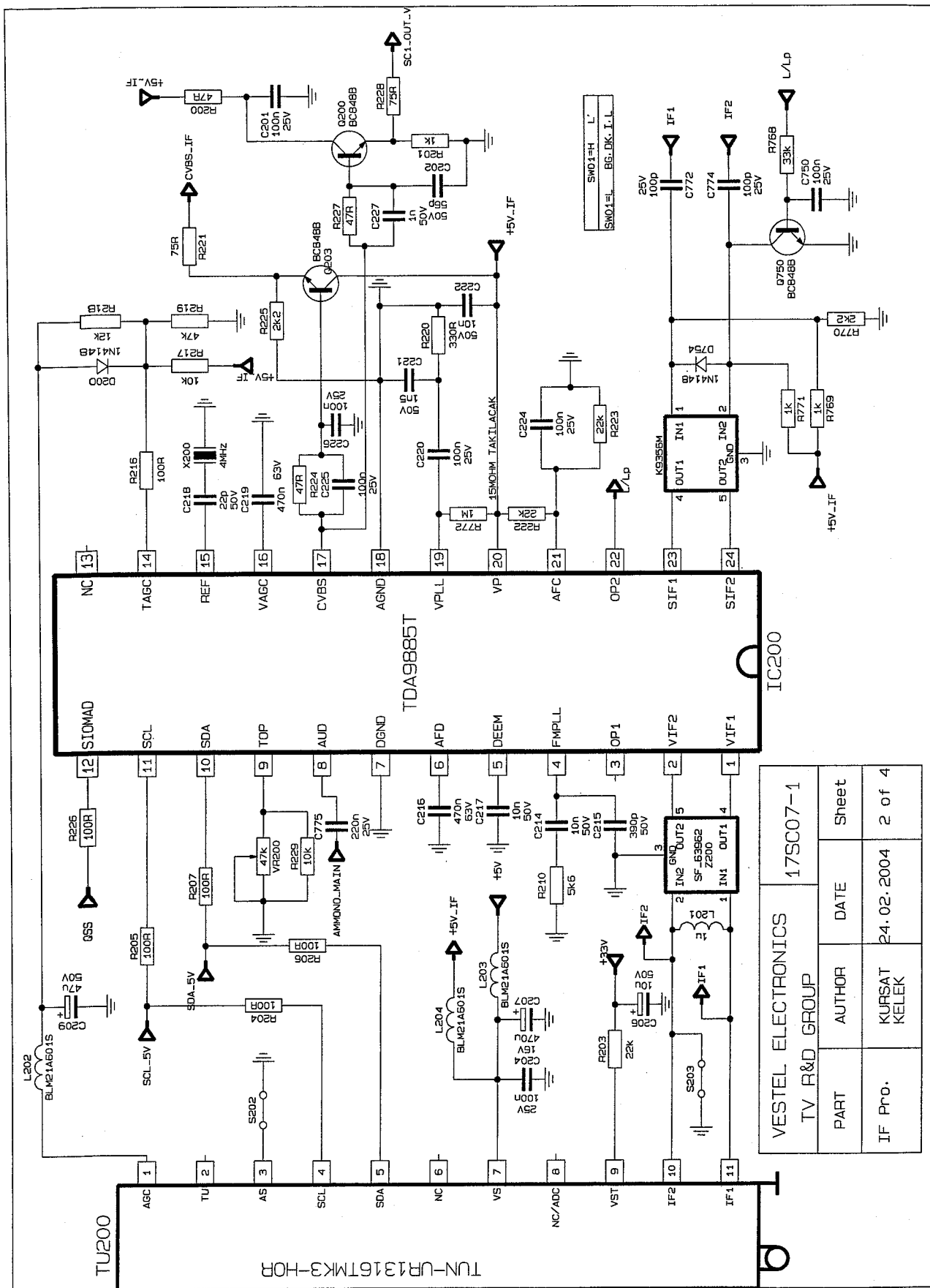
|                    |              |            |        |
|--------------------|--------------|------------|--------|
| VESTEL ELECTRONICS |              | 17SC07-2   |        |
| TV R&D GROUP       |              | DATE       | Sheet  |
| PART               | AUTHOR       | 23.05.2003 | 1 of 4 |
| Video Pro.         | KURSAT KELEK |            |        |



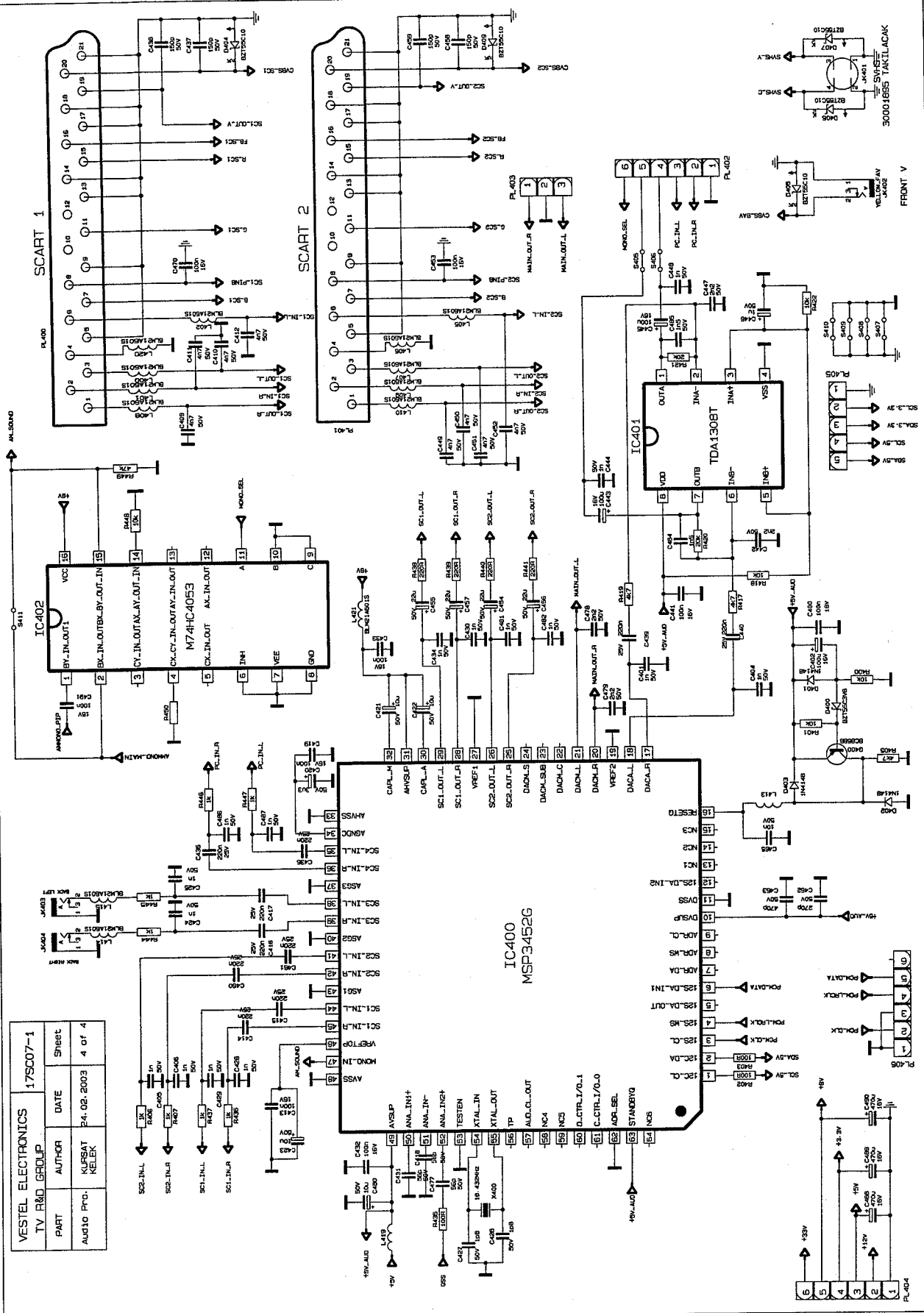


|                    |            |        |
|--------------------|------------|--------|
| VESTEL ELECTRONICS |            | 17MB07 |
| TV RMO GROUP       | SHEET      |        |
| PART               | DATE       |        |
| 10000181           | 12.12.2002 | 2 of 2 |
| KUFSAT             |            |        |
| KELER              |            |        |





|                    |        |            |
|--------------------|--------|------------|
| VESTEL ELECTRONICS |        | 17SC07-1   |
| TV R&D GROUP       |        |            |
| PART               | AUTHOR | Sheet      |
| AUG10 PTD.         | KJRSAT | 24.02.2003 |
|                    | KELEK  | 4 OF 4     |



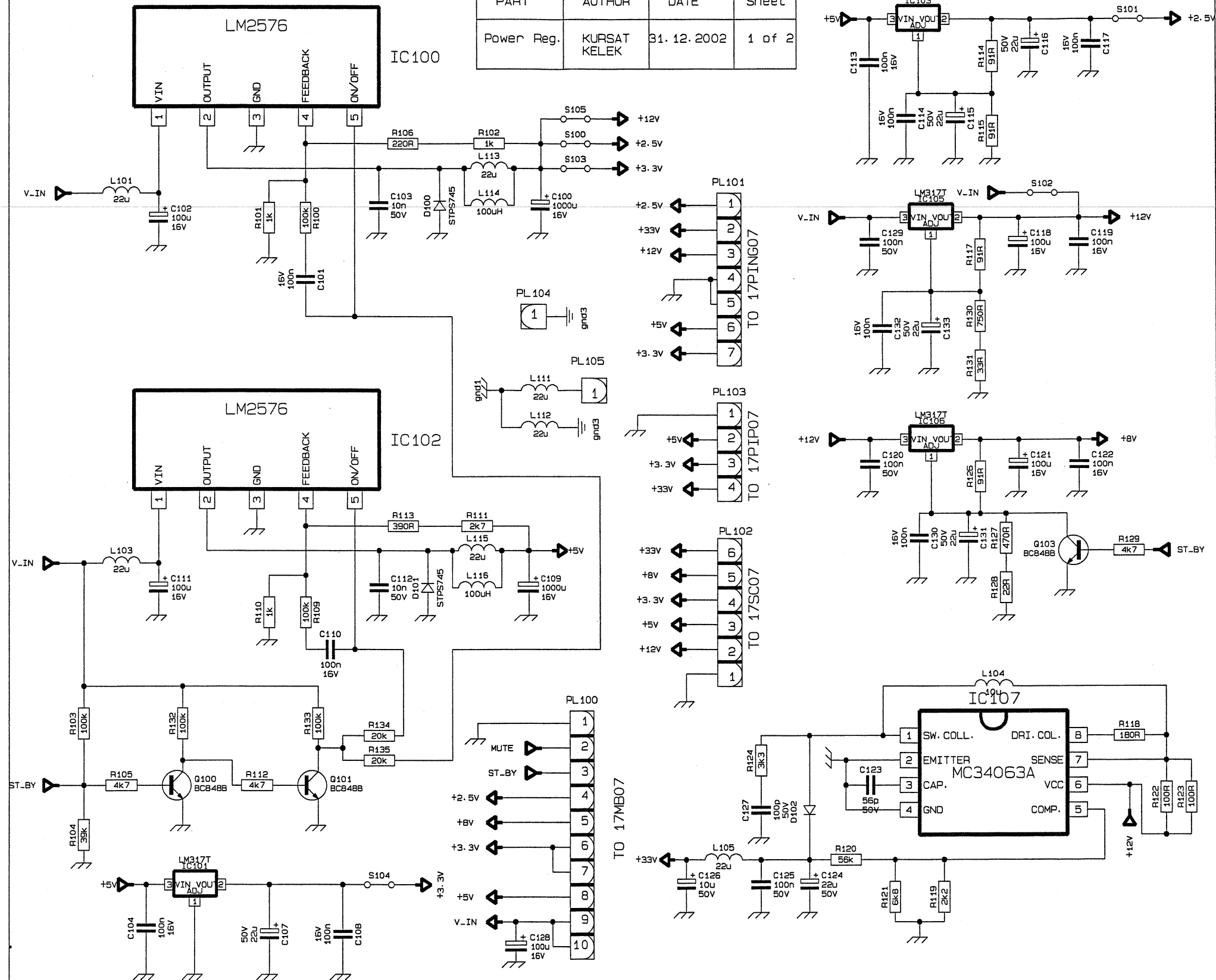
30001855 TAKILACK

FRONT V





|                    |              |            |        |
|--------------------|--------------|------------|--------|
| VESTEL ELECTRONICS |              | 17AMP07    |        |
| TV R&D GROUP       |              |            |        |
| PART               | AUTHOR       | DATE       | Sheet  |
| Power Reg.         | KURSAT KELEK | 31.12.2002 | 1 of 2 |



A

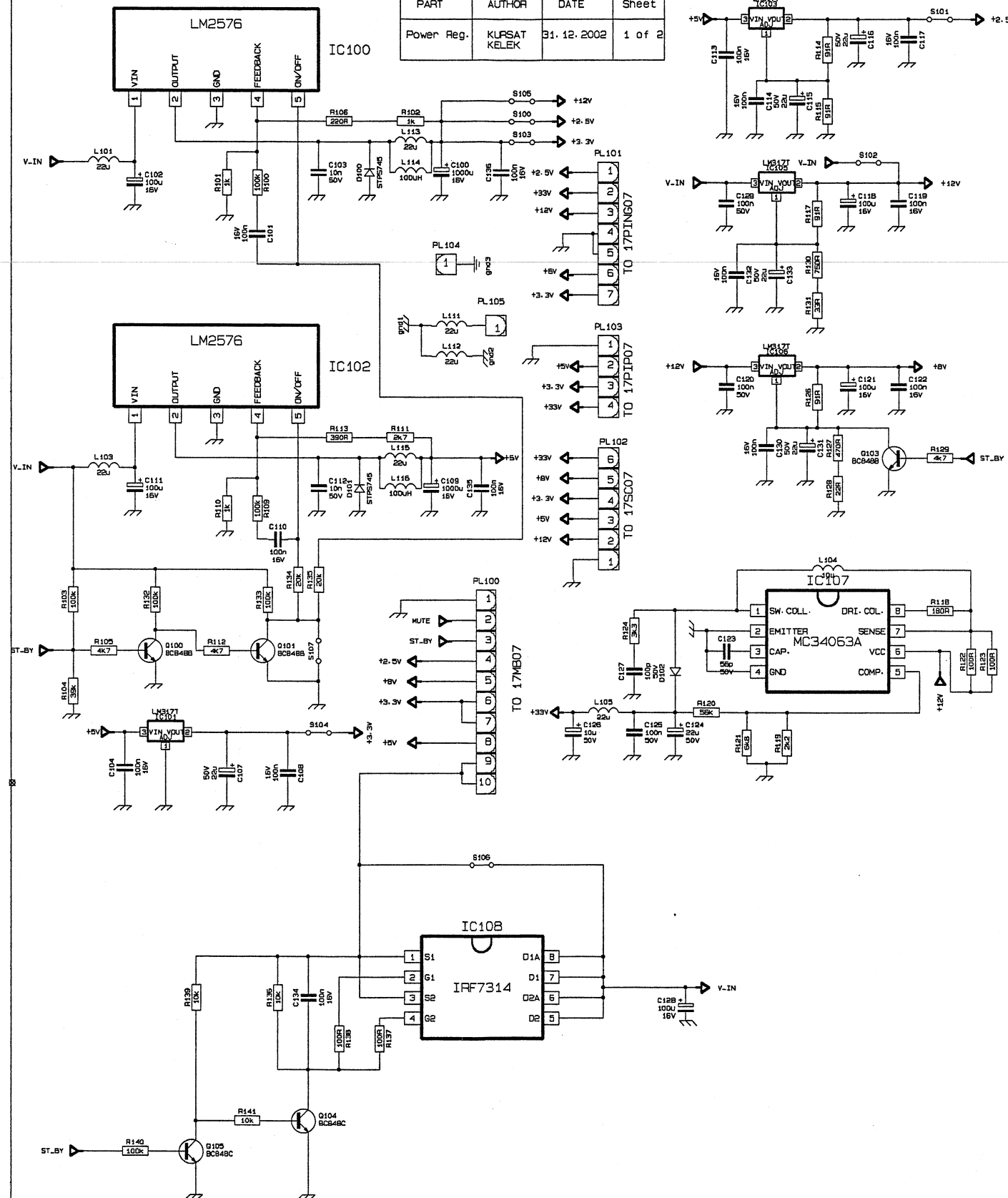
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C

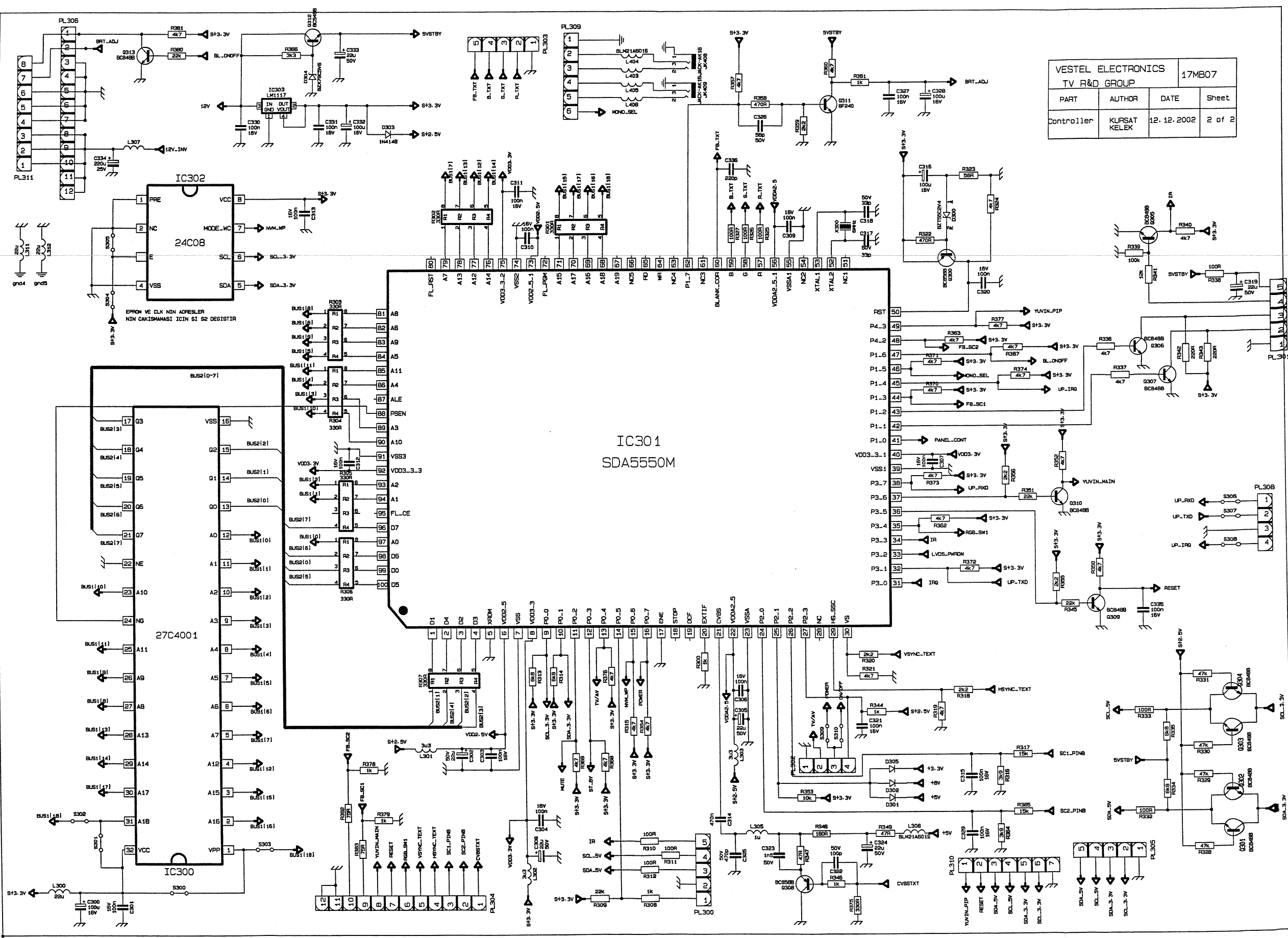
D

E

|                    |              |            |        |
|--------------------|--------------|------------|--------|
| VESTEL ELECTRONICS |              | 17AMPO7    |        |
| TV R&D GROUP       |              | Sheet      |        |
| PART               | AUTHOR       | DATE       | 1 of 2 |
| Power Reg.         | KURSAT KELEK | 31.12.2002 |        |



|                    |              |            |        |
|--------------------|--------------|------------|--------|
| VESTEL ELECTRONICS |              |            | 17MB07 |
| TV R&D GROUP       |              |            |        |
| PART               | AUTHOR       | DATE       | Sheet  |
| Controller         | KURSAT KELEK | 12.12.2002 | 2 of 2 |



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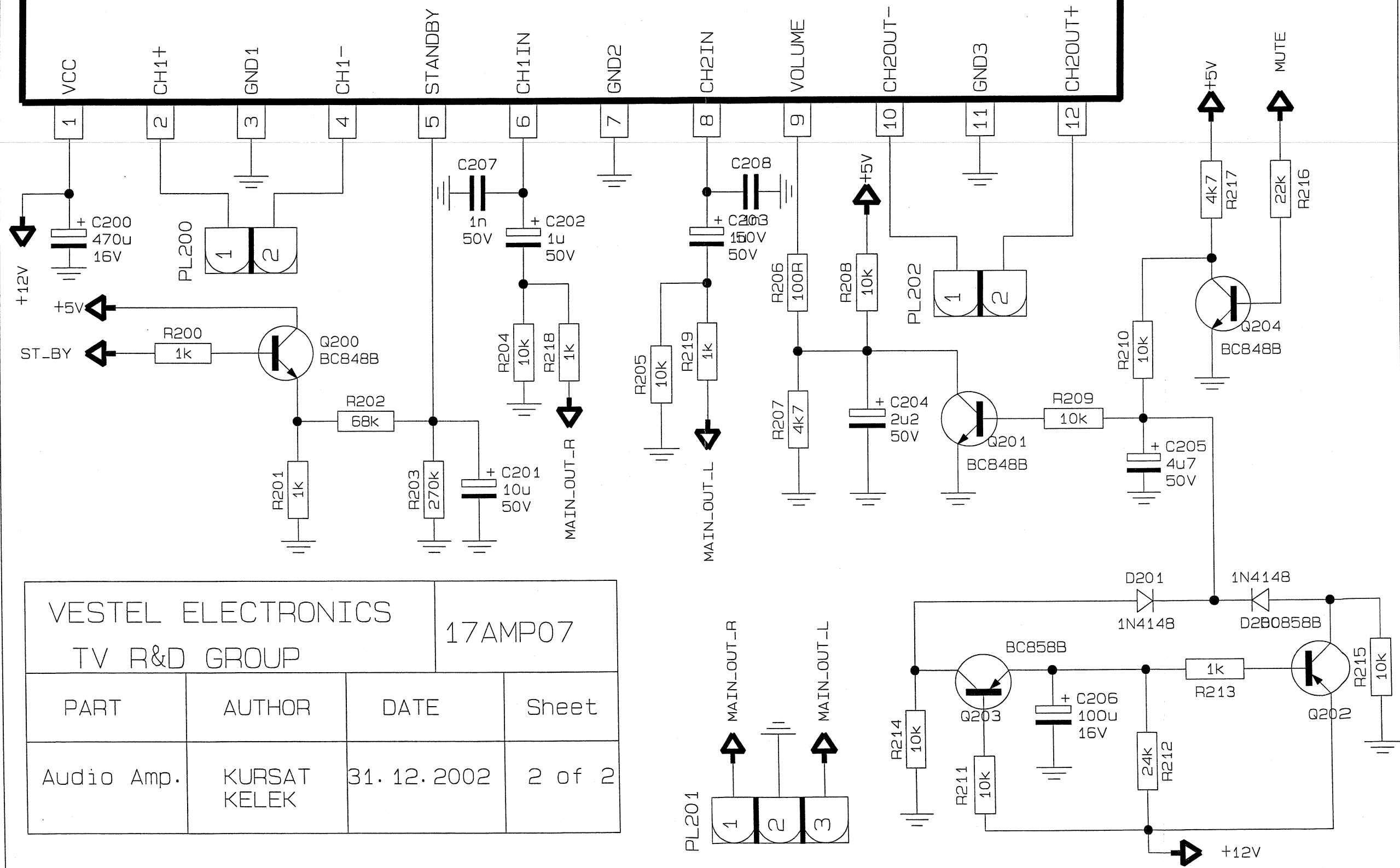
4

5

6

IC200

AN7522N



|                    |              |              |         |
|--------------------|--------------|--------------|---------|
| VESTEL ELECTRONICS |              |              | 17AMP07 |
| TV R&D GROUP       |              |              |         |
| PART               | AUTHOR       | DATE         | Sheet   |
| Audio Amp.         | KURSAT KELEK | 31. 12. 2002 | 2 of 2  |

A

B

C

D

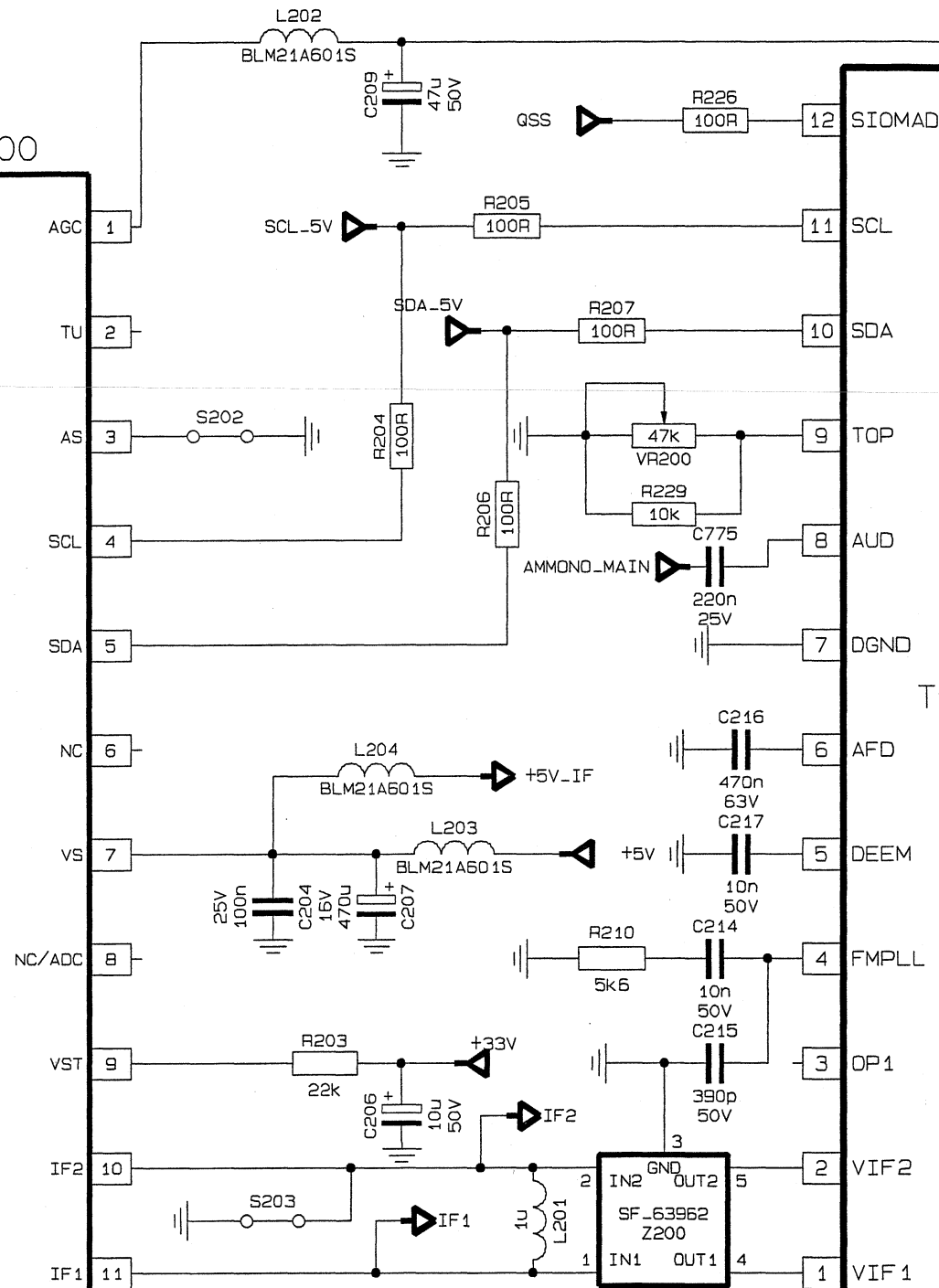
1

2

3

TU200

TUN-UR1316TMK3-HOR



VESTEL ELECTRONICS  
TV R&D GROUP

17SC07-2

PART

AUTHOR

DATE

Sheet

IF Pro.

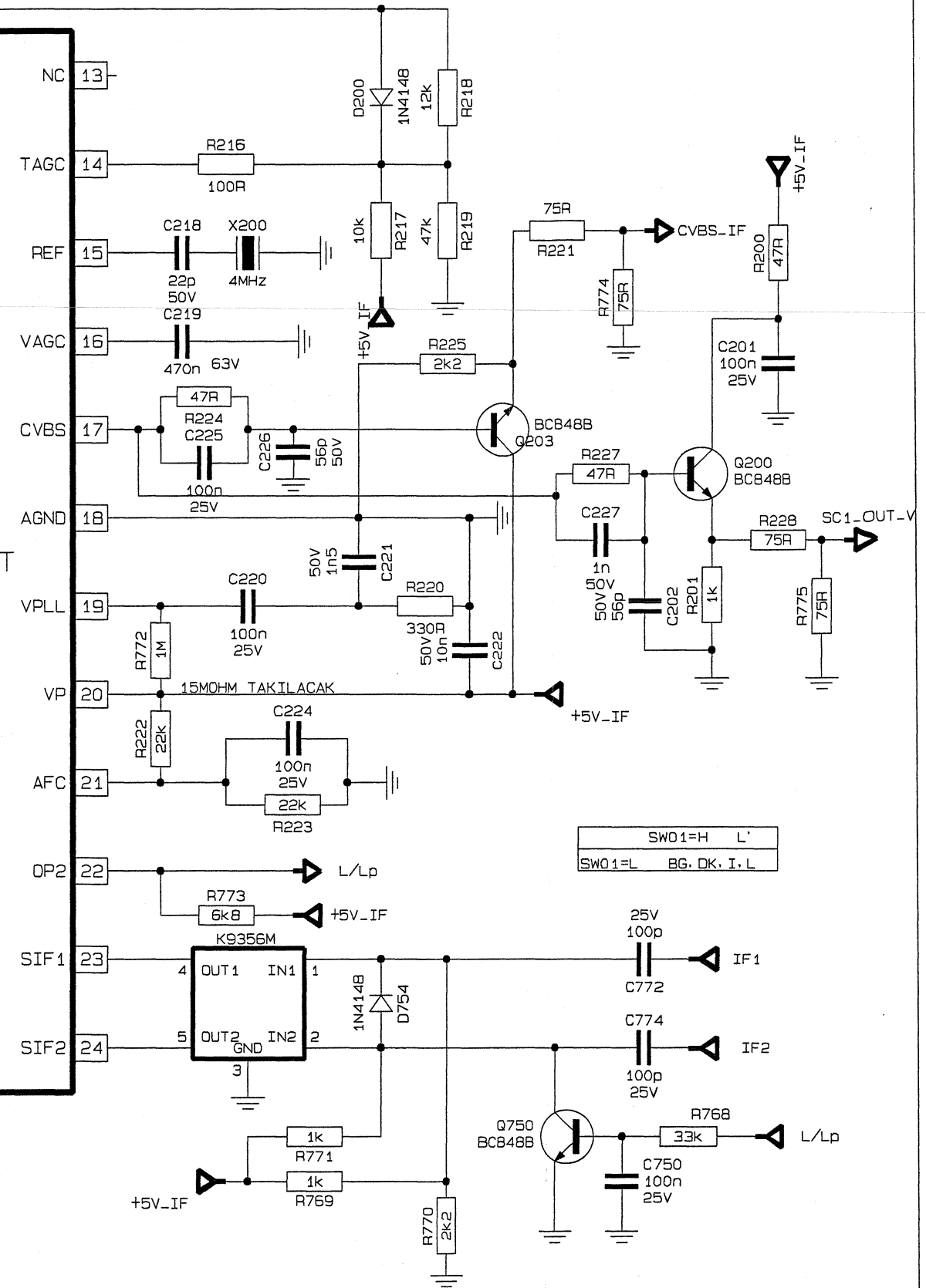
KURSAT  
KELEK

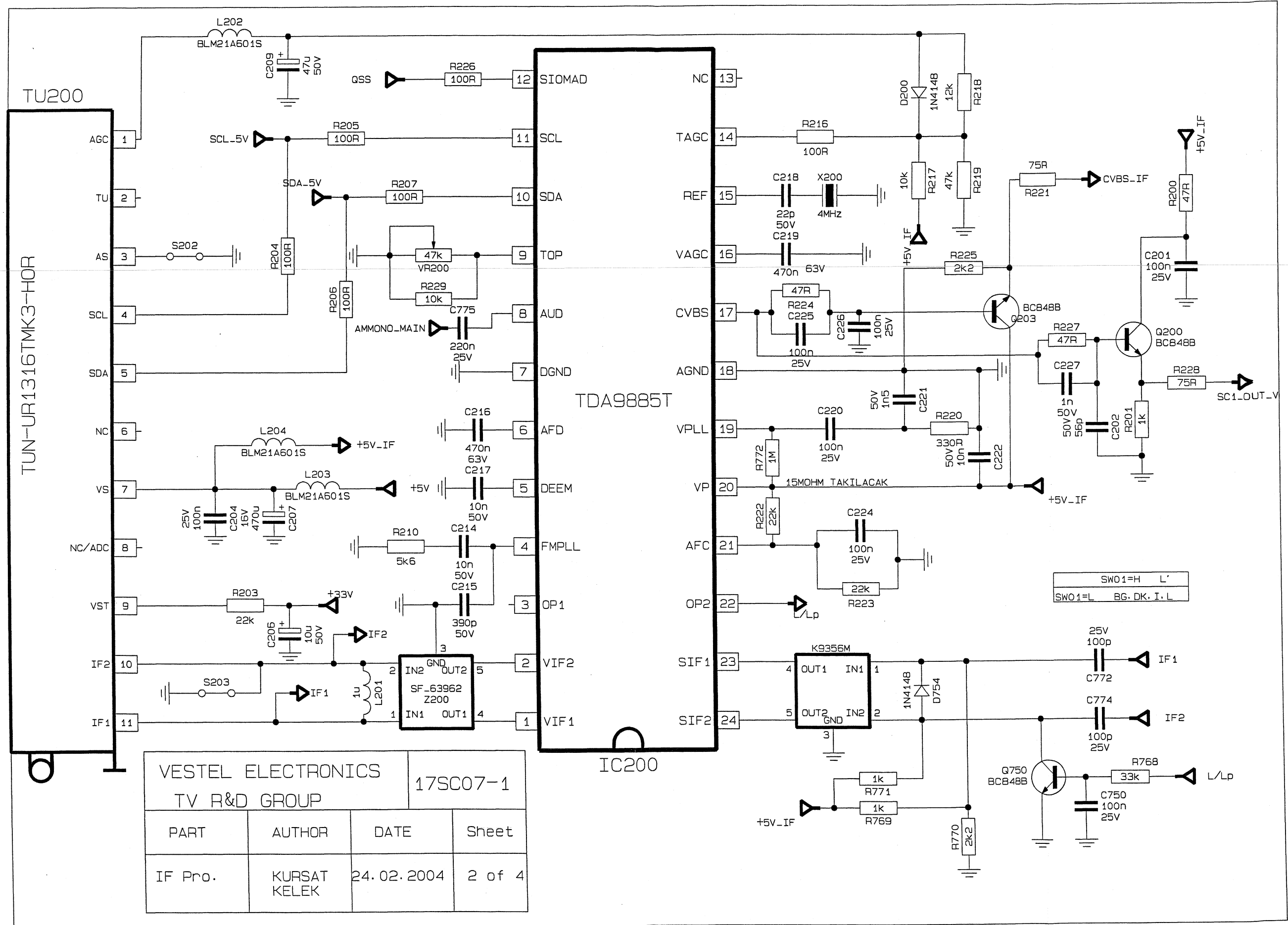
23.05.2003

2 of 4

TDA9885T

IC200





|                    |              |            |        |
|--------------------|--------------|------------|--------|
| VESTEL ELECTRONICS |              | 17SC07-1   |        |
| TV R&D GROUP       |              |            |        |
| PART               | AUTHOR       | DATE       | Sheet  |
| Audio Pro.         | KURSAT KELEK | 24.02.2003 | 4 of 4 |

